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POLYMER LIGHT-EMITTING DIODE (PLED) PROCESS DEVELOPMENT

by

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14. ABSTRACT
This report documents the effort and results of process development leading to a direct driven polymer light-emitting diode (PLED) display on a flexible substrate manufactured on roll-to-roll line. The challenge was twofold: i) to design and fabricate PLED specific NanoBlock integrated circuit (IC) for current driven display devices, and ii) to integrate very sensitive PLED processes (in terms of morphology and topography) with a back plane having embedded NanoBlock ICs under the PLED active area. Each NanoBlock IC provides eight independent constant current supplies for eight display pixels with capability of 4 bit gray scale. The development of integrated NanoBlock IC back plane is described in detail including the description of final optimized structure. The successful integration is documented on a segmented display driven by six NanoBlock ICs embedded in the display back plane. The results are compared with the goals of the Task 1.1.5. Also the effort to identify a web compatible coating technology for PLED materials is also provided. The report is closed with a summary of conclusions and recommendations for Phase II of the Flexible Display Program.

15. SUBJECT TERMS

LIGHT EMITTING DIODES	LIQUID CRYSTAL DISPLAY SYSTEMS	POLYMERS
FLAT PANEL DISPLAYS	INTEGRATED CIRCUITS	PIXELS
NANOBLOCK(TRADEMARK)	DISPLAY SYSTEMS	SUBSTRATES
FLUIDIC SELF ASSEMBLY	PLED(POLYMER LIGHT EMITTING DEVICE)	LUMINANCE

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Contents

Contents (continued)

Contents (continued)

Contents (continued)

Contents (continued)

Contents (continued)

LIST OF FIGURES

LIST OF TABLES

PREFACE AND ACKNOWLEDGEMENTS

This report represents one of the deliverable components for Defense Advanced Research Projects Agency Contract DAAD 16-00-C-9234 which was awarded to Alien Technology Corporation on March 01, 2000. Alien Technology Corporation was chosen to participate in the Flexible Display Program because its proprietary Fluidic Self-Assembly of NanoBlock™ ICs into a plastic substrate showed a great promise in delivering most of the flexible display attributes as specified in the BAA 99-17. The research program covered the period March 2002 through September 2002.

Most of the attributes were to be demonstrated by utilizing already established Liquid Crystal display technology in combination with the new NanoBlock backplane for direct-driven matrix displays.

Moreover, it was recognized that there is great synergy achievable by integration of Fluidic Self Assembly on plastic substrates with another emerging flat panel display technology known as Organic Electroluminescence. As such, part of the DARPA Contract supported development of processes that would demonstrate feasibility of integration of a display backplane incorporating NanoBlock ICs and organic light emitting diode technology. Since the organic LED technology chosen was based on polymeric emitters, we refer to these devices as PLED devices.

The deliverable described in Task 1.1.5 of SOW 991217 Rev-H is “A report detailing the process development results, the planned manufacturing flow for PLED displays and the ability to achieve the program’s brightness and efficiency goals.” This report constitutes the deliverable for the Task 1.1.5.

The goals for Phase I (Baseline Program) were set to achieve brightness of 150cd/m^2 and efficiency of 0.3 lumens/Watt. The goal for Phase II was to extend this basic performance into a high-resolution flexible display device.

The Contract was renegotiated during 1999 so that Alien Technology Corporation became the main contractor and EEES of Northrop Grumman and Dow Chemical Company became subcontractors. The Contract was terminated by DARPA in July 2002, on the grounds of convenience.

ACKNOWLEDGMENTS

Authors are grateful for the financial support provided by DARPA Flexible Display Program. Our thanks go to members of PLED Group at Alien Technology Corporation for their dedicated work on process development and fabrication of PLED displays. We would also like to thank Eric Forsythe and David Morton at Army Research Laboratory for their analytical studies of our PLED samples.

PLED PROCESS DEVELOPMENT FOR
DARPA FLEXIBLE DISPLAY PROGRAM

SUMMARY

The focus of this effort was to demonstrate the feasibility of integrating two emerging flat panel display technologies – flexible electronic backplanes produced by Fluidic Self-Assembly (FSA) of tiny integrated circuits known as NanoBlock ICs, and organic electroluminescent displays.

The challenge of combining two emerging technologies is quite formidable, but so is the potential synergy that could lead to flexible Polymer Light Emitting Diode (PLED) displays driven by embedded NanoBlock ICs. The capabilities of NanoBlock ICs allows for highly-optimized CMOS circuitry, providing practically identical local current sources required for achieving uniform luminance of the PLED pixels across the display area. In contrast, conventional active matrix arrays utilizing poly-crystalline silicon thin film transistors (TFT) on glass substrates typically show uniformity problems when applied to PLED displays. These problems become even more severe when the TFTs are fabricated on a plastic substrate, severely limiting the processing temperature during fabrication.

In Phase I of the program, we demonstrate how a direct drive NanoBlock IC backplane offers many advantages for PLED displays:

- The capability to drive all pixels in a direct drive manner. This addressing scheme can be applied to segmented as well as to a matrix display. By driving the PLED pixels directly, it is possible to achieve higher efficiency than passively driven displays as the pixels don't need to be driven at high, transient light output levels.
- The uniformity of output current of devices made on crystalline silicon will be in vicinity of ±1% compared to a typical TFT uniformity of ±10% within the display area.
- The manufacture of NanoBlock ICs in a plastic substrate is a promising alternative to the construction of polysilicon TFTs on plastic substrates.
- As the FSA process is compatible with the roll-to-roll manufacturing, the economy of manufacturing flexible PLED displays can be further increased by the sheer efficiency of web processing.

In Phase II of the program, we began work on extending the Phase I work towards high pixel count PLED displays:

- Work was begun on passive row and column NanoBlock IC drivers that could provide a near-term route to practical high pixel count displays in a flexible display form factor
- Work begun on the development of flexible barrier materials suitable for protecting PLED devices and be compatible with NanoBlock IC device structures.

The PLED-specific NanoBlock IC has been designed at Alien Technology Corporation and manufactured at AMI, a semiconductor foundry in Pocatello, ID. It has eight regulated current outputs (each 175 μA max) capable of 16 levels of gray scale. After testing at the foundry, the wafers were then shipped back to Alien for singulation. Some of the PLED-specific NanoBlock ICs have been encapsulated in a standard package for further characterization. The testing confirmed that the NanoBlock ICs respond to command and data streams and produce output current as designed. The uniformity of the output currents was somewhat lower than expected, but still respectable at ±1.5%.

To address the integration issues we first established the in-house capability to produce PLED devices. Alien acquired a set of equipment needed for PLED device fabrication (PLED line) and installed it in Class 100 cleanroom. The core of the PLED line consists of three pieces of equipment: a spinner, a custom made evaporator, and a glove box with inert atmosphere. The evaporator and glove box are integrated: i.e. the processed device can be directly transferred from the evaporator in the glove box without exposure to oxygen and/or water present in air. This is an important capability, as both air and water have severe detrimental effects on PLED devices.

The first task was to develop a Baseline Process for making PLED device on glass substrates coated with commercial Indium Tin Oxide (ITO) film. We have designed two simple structures on one substrate to serve this first task; we call this unit Test Vehicle 1 (TV-1). Within three month after the equipment installation we were able to produce PLED devices with enough brightness and long enough life to be suitable for the feasibility study of the integration issues.

We proceeded with fabrication of devices made on ITO/glass, but this time the ITO film was deposited in Alien's sputtering machine. Again, in a short time we successfully produced working PLED devices on our TV-1 substrates.

The next step was to fabricate our PLED TV-1 structures on a substrate that would be similar to the type of electronic backplane that would contain NanoBlock ICs. This was an important consideration, as many type of receptor substrates useful for NanoBlock ICs will have an embossed or cast plastic coating to contain the NanoBlock ICs. For this phase, glass substrates were coated with plastic material, Norland Optical Adhesive. This system is used in one of Alien's standard manufacturing processes to produce integrated NanoBlock IC backplane for liquid crystal displays (polymer dispersed liquid crystal displays). We found that the Norland Optical Adhesive surface was incompatible with PLED processing and needed to be replaced.

We have identified the important characteristics that the backplane surface must have to satisfy the many requirements coming from both FSA and PLED processing. This surface must serve several purposes:

- act as a suitable material for NanoBlock IC receptor sites
- serve as a material for press- and spin-planarization of the NanoBlock ICs, and
- provide a flat, stable and defect -free support for PLED structures.

Rather than attempt to design and develop a customized polymeric coating, we opted for screening commercially available polymers and epoxies. After extensive examination of 23 materials in a three-stage screening process, we identified four promising candidates. Each of these materials was optimized for its particular function within the NB backplane.

The TV-1 system served its purpose for initial screening. For the next stage of integration, this system was replaced by the Test Vehicle 2 (TV-2), consisting of embedded NanoBlock ICs in the active area of the test displays. Apart of many test structures, there are two kinds of displays in each TV-2: a segmented one, with six NanoBlock ICs per display, and a matrix display, having 48 NanoBlock ICs. The direct drive scheme was used as addressing technique for both displays. The purpose of the TV-2 was to act as an intermediate platform towards higher pixel density displays.

At the end of the Phase I (Basic Program) we have just resolved the main issues of the integration, and produced first displays showing emission from pixels driven by the PLED-specific NanoBlock ICs. The light generated in the pixels of matrix displays surpassed the goals in brightness and efficiency as stated in the program SOW (150cd/m2 and 0.3 lm/W). However, we did run into problems with the control of displayed images, having to do with both electronic and interconnect issues.

A second aspect of the program was the examination of coating processes that could lead to high volume PLED device construction. As such, in parallel to the above efforts on the integrated NB backplane, we were also screening coating techniques suitable for deposition of PLED materials in roll-to-roll manufacturing environment. After a review of available techniques we decided to concentrate on two: slot die coating and offset gravure printing. Slot die coating is a noncontact coating process known for its ability to apply optically uniform thin coatings for a variety of industries. Offset gravure was chosen because of its capability to induce a shear within the coated material during the coating process, which seems to best mimic the coating conditions of the already established coating technique, i.e., spinning. Of course, we were aware of inkjet technology being successfully used for color PLED displays, but we felt the inkjet technique is too cumbersome and slow for manufacturing of monochrome PLED displays.

We can report substantial success with the slot die coating. After several trial runs we were able to build functional TV-1 devices on rigid as well as on flexible substrates. We consider this achievement a technological breakthrough, as we are not aware of any other such successful demonstration of slot die coating of PLED devices. This technology is ideally suited for economical production of monochrome PLED displays in large volume. For completeness, we note that the offset gravure tests ran into difficulties during the trial runs at vendor site.

In anticipation of transferring our technology from glass to plastic substrate, we started to test barrier layers from two suppliers (barrier layer protects the PLED materials from an ingress of oxygen and water through the plastic substrate; a hermetic packaging is neces-

sary for preventing fast degradation of PLED device). We used a “lid test” on our TV-1 devices, i.e., we replaced a glass lid with the plastic one having barrier layer(s) deposited on one or both surfaces. While not all samples performed well in the lid test, certain multi-layer barriers form Vitex Systems were comparable to glass in their ability to protect the test devices from the environment. We thus proceeded to use the Vitex System’s barriers for the work for Phase II.

Nevertheless, the patterning of Vitex materials was problematic for NanoBlock IC designs. This difficulty led to the in-house development of an alternative approach towards barrier materials. This internal barrier coating work is detailed later in this report.

The experience gained through the Phase I development work has been distilled in two new designs: i) a simplified NB backplane with two barrier layers integrated into a PLED structure, where one barrier layer serves as planarization layer as well, and ii) an integrated backplane for passive matrix PLED displays driven form the edges of the display by embedded NanoBlock IC row and column drivers.

Asides from the control issues, we have demonstrated the basic compatibility of PLED devices on FSA NanoBlock IC backplanes. At the time of termination, the following development efforts were underway:

- A focused thrust on passively-addressed PLED displays. Passive PLED displays offer a rapid path towards high pixel count displays, which is in line with Alien’s commercial activities.
- Development of high-performance NanoBlock ICs for row drivers and for column drivers for PLED displays
- Deployment of these row and column NanoBlock ICs in plastic “driver strips”, which can be attached to and drive passive displays made by other companies
- Integration of these row and column drivers into a backplane that will be integrated into a PLED display.

Successful completion of these tasks would have servde as a near-term springboard towards devices that have both defense and commercial applications.

- These NanoBlock IC driver strips can be integrated into existing glass or plastic OLED or PLED displays made by other companies. Aside from significant cost advantages, these “flexible drivers” can add additional durability and flexibility to plastic based displays.
- Integrated NanoBlock IC backplanes (with the NanoBlock IC in the plastic backplane itself) will offer further advantages in durability and form factor for organic emissive displays. Such an integrated backplane can serve as a springboard towards a “tiled passive” display array. An array of passive displays built into a backplane could conceivably provide the high pixel counts of active matrix displays without the cost and difficulty of polysilicon backplanes.

1. INTRODUCTION

Organic light-emitting diode (OLED) displays are attracting an enormous amount of worldwide development as a next-generation flat panel display technology. Both displays based on small molecule emitters and polymer emitters (the latter sometimes called PLED displays) are under development. Remarkable progress has been made in producing both passively addressed and active matrix-addressed displays.

Despite this attention, several severe challenges remain for this display technology. The incredible sensitivity of OLED/PLED display components to water and to oxygen has mostly restricted these displays to carefully packaged glass displays. To achieve high pixel counts, expensive and difficult-to control-polysilicon TFT technology appears necessary for the backplane. OLED/PLED displays require high currents, polysilicon technology is challenging to make uniform across a display, and polysilicon TFTs on plastic substrates is still in an early developmental stage

Alien NanoBlock IC technology offers numerous advantages for emissive organic displays, and offers an alternative approach towards advanced OLED/PLED displays. NanoBlock ICs can be constructed from single crystal silicon using standard CMOS processes. The NanoBlock ICs, once deployed into a substrate and built into a PLED display, can provide high, uniform currents to drive these emissive displays. The NanoBlock ICs can be deployed in plastic substrates, enabling flexible, lightweight, and durable displays. The FSA process pioneered by Alien provides for the rapid and inexpensive assembly of NanoBlock IC into backplanes, providing cost advantages for these displays.

For further discussion within this report we assume that the reader has a basic understanding of OLED/PLED technology. Good introductory tutorials can be found on the web site of Cambridge Display Technology[1], or at the web site of the Eastman Kodak Company[2].

The scope of work for the Phase I of the program has been defined with several thoughts in mind:

- Alien is developing its proprietary NanoBlock ICs and FSA processes for use in displays for both commercial and defense applications. For this first phase, Alien will employ its novel direct drive addressing scheme for the PLED display.
- Alien is not currently a manufacturer of PLED displays. The determination whether to enter in such business (directly or via joint venture), or to supply NanoBlock IC components to other display manufacturers, will be made after completion of the Phase I and II.
- The current construction of NanoBlock IC backplanes (NB backplanes) will likely be different after introduction of plastic films with preformed receptor sites in 2001/2002. As such, the goal of the project is to demonstrate basic compatibility

[1] http://www.cdtltd.co.uk/
[2] http://www.kodak.com/US/en/corp/display/index.jhtml

between NanoBlock ICs and PLED technology, recognized that advanced technology will be available for future development and commercial work.

In Phase I we aimed to prove that it was possible to successfully integrate Nanoblock IC and PLED technologies by the development of processes for fabrication of functional samples. While basic compatibility will be shown, it was not the intent of this Phase I work to deliver processes suitable for manufacturing of PLED displays. Rather we concentrated on understanding the challenges of the integration and of the new direct drive addressing technique when applied to PLED media.

Our investigation followed three main themes:

- The design and construction of a NanoBlock IC useful as a constant current supply for PLED displays
- The integration of NanoBlock IC backplanes with PLED displays
- A feasibility study into roll-to-roll coating technologies that would support the switch from sheet substrate to web.

While the goal of Phase I is to show basic compatibility between NanoBlock IC and PLED technologies, Phase II was aimed at enabling high pixel count emissive displays employing NanoBlock ICs. Phase II was aimed at demonstrating passively-addressed PLED displays with NanoBlock ICs. The NanoBlock ICs will be deployed both as a discrete, flexible unit, or embedded into the display backplane. This development work would enable NanoBlock IC technology to be applied to OLED and PLED displays manufactured outside of Alien, as well as provide a route towards novel passive displays with embedded NanoBlock ICs. The boundaries of the workspace for Phases I and II are shown in Figure 1.

A major challenge for this work is to provide compatibility of NanoBlock ICs in the display's active area with the PLED materials. Presently, NanoBlock ICs deployed in a substrate tends to produce bumps several μm high on the surface of the last planarization layer. Unexpectedly, we also run into problems associated with cleanliness of ITO surface, which had a profound effect on the quality of fabricated devices.

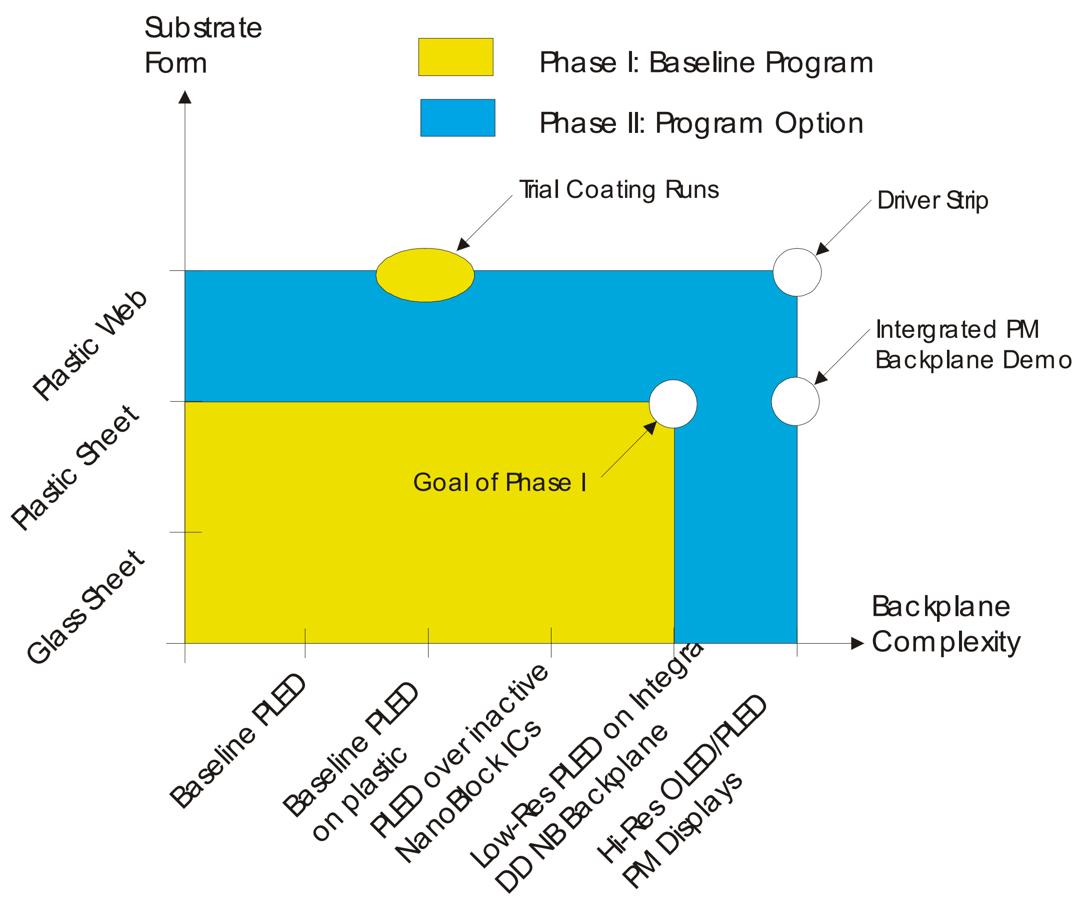


Figure 1. The work space for Phase I and II confined by backplane complexity and substrate form.

The contamination of the ITO has two root causes. The plastic sheets we used did not allow certain cleaning steps, as they are not resistant to solvents. Additionally, these plastics can release chemical species (either its own components or trapped liquids from wet processing) from their surface over time.

We decided to establish a basic capability to produce PLED devices in house that gave us fast turnaround and good control over the integration issues. The light emitting polymers used in this work were Green B and Green K emitters from Dow Chemical. From time to time we had to revisit the basic PLED recipe as the improvements in the light emitting materials required re-optimization of our PLED processes.

Our efforts to demonstrate web coating for PLED devices was motivated by the need to demonstrate an efficient, low-cost means of producing monochrome displays on plastic. Such displays are highly compatible with NanoBlock IC backplanes, and could be of future commercial and defense interest. While web coating is well-established art, the coating of PLED materials with the necessary thickness and uniformity is a great challenge. Both layers in question, the hole transport layer and light emitting polymer layer, are of

thickness well below the common range within which the converting industry operates. Nominal thickness of both PLED layers is 80 nm. In addition, both layers are deposited from solutions having only 1% of solids, which translates in low viscosity and drying problems.

The web related activities needed to be carried at vendor sites in the form of trial coating runs. Despite some serious issues in using coating equipment outside of cleanrooms, and logistical problems with sample transport, we were successful in demonstrating slot die coating as a suitable replacement for the standard spin casting technique.

A basic challenge we attacked was the nonuniformity issue often found in PLED displays. PLED displays are unusual current driven devices, and it presently known that standard active matrix designs having two to four thin film transistors per pixels have great difficulties in delivering the same current to each PLED pixel. This difficulty tends to produce OLED/PLED displays with obvious luminance nonuniformities (*i.e*., a "pepper and salt" look). A PLED specific NanoBlock IC was designed to address this issue. Our PLED NanoBlock IC incorporates a 4 bit (16 level) gray scale in order to demonstrate the high degree of control achievable by NB backplanes.

2. HARDWARE

To support development activities through the Baseline Phase of the DARPA program, it was necessary to acquire a set of equipment for establishing a PLED processing capability (PLED Line), as well as needed equipment for testing and evaluation of the produced PLED devices.

2.1 PLED Line

At the onset of this work we determined the need for an in-house capability to produce PLED structures at least at a rudimentary level. The list of the equipment deemed necessary was based on the recommended process flow we received from Dow Chemical, who served as our supplier of the Light Emitting Polymer (LEP). For description of the process please see Appendix A. The PLED Line consists of following equipment: Cleanroom HEPA filtered oven (VWR), spinner (Karl Suss), Class 10 flow module (Universal), thermal evaporator (Kurt J Lesker), and glove box (MBraun). The choice of vendors was guided by the recommendations provided by Dow Chemical and UCLA, both with proven capability to produce PLED devices. Our equipment has the capability to process 6"x 6" sheet substrates, either glass or plastic. The original conceptual design of the

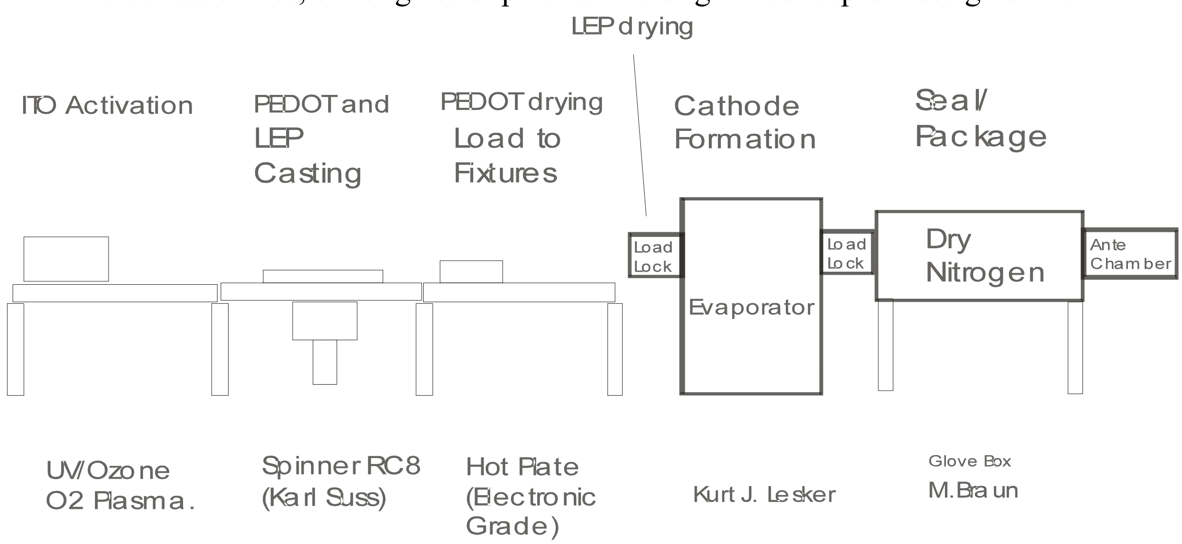


Figure 2. Conceptual drawing of PLED Line

PLED line (Figure 2) was influenced by reviews of already existing application laboratories at Dow Chemical, UCLA and Covion. The process flow was designed to proceed from left to right in Figure 2, so that after encapsulation in the inert atmosphere at the glove box, the completed device can be taken out to air.

The major advantage of our PLED Line compared to other PLED labs was the integration of the evaporator with the glove box, so that the incomplete samples were not exposed to air before encapsulation. The custom made evaporator was designed to handle up to 6"x 6" substrates, a target size for sheet substrates of Alien backplane pilot line. Substrates

are dropped in a shadow mask fixture and loaded through an entry loadlock, which allows a bake of the PLED structure under high vacuum. Cryopumps for all three chambers (main chamber and two loadlocks) were chosen for their capability to pump water vapor to a very low partial pressure in order to minimize entrapment of water molecules in the fabricated PLED device. The uniformity of deposited metallic layers (cathode) was better than ±5% due to rotation of substrate holder. After completion of the evaporation cycle, the sample was transferred from the main chamber through an exit load lock directly into the glove box filled with dry nitrogen (oxygen and water vapor kept below 2 ppm) to complete the device encapsulation.

All the above equipment was installed in an Alien Technology class 100 cleanroom and occupies about 250 ft^2. (Alien's cleanrooms consist of three bays of Class 100 and one bay of Class 10,000). Figure 3 shows a photograph of completed PLED Line after installation. Some improvements were done later, such as installation of a laminar flow hood with Class 10 filtration unit to prevent particle contamination of processed PLED devices. It should be noted that the delivery of the KJL evaporator was delayed by six months due to vendor problems, but the availability of another evaporator located in the Alien cleanroom mitigated most of the impact on the PLED development work.

Figure 3. PLED Line after installation. Left: HPEA oven, spinner, and Class 10 flow hood. Right: Custom made evaporator and glove box.

2.2 Life Test Rack

Many defects in the PLED devices, such as black spots, brightness decay, *etc.*, become more obvious after days or months of operation. We established a rudimentary life testing capability in Alien's warehouse by populating a commercially available rack with ten boxes that serve as constant current sources. Each box can drive independently up to ten PLED devices. These constant current sources (PLED drivers) were designed and built by Alien. The view of one shelf in the test rack containing 3 constant current sources is shown in Figure 4. The rack has five shelves.

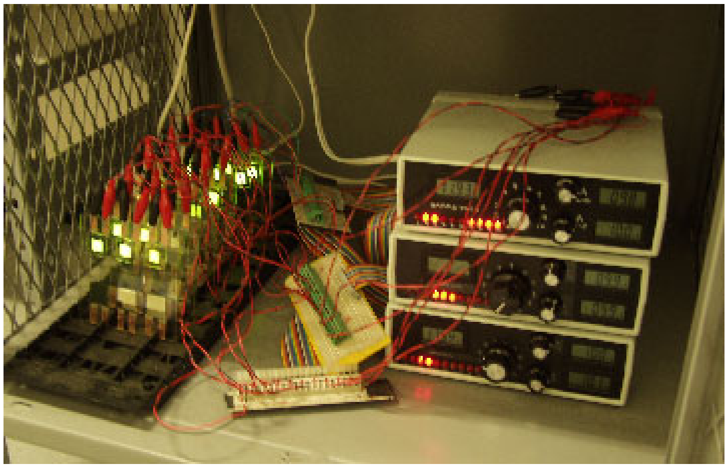


Figure 4. Life testing: one shelf with devices under test.

2.3 Electro-Optical Characterization of PLED Devices

An important aspect of our work with various deposition techniques is to evaluate the electro-optical performance of these devices. To evaluate our PLED devices, we acquired a spectro-photoradiometer SpectraScan 705 manufactured by Photo Research Corporation. This instrument is a workhorse within the flat panel display industry. This instrument was critical in establishing the performance of both the baseline PLED process and PLED devices fabricated on integrated NB backplanes. The spectrophotometer was later incorporated into a semi-automated display characterization system , FPM 500, made by Westar Corporation (Figure 5.). This configuration will not only provide the basic information about the electro-optical performance and spectral distribution of emitted light, but can also measure the same characteristics at each pixel along both vertical and horizontal axes.

This instrument was critical in establishing the performance of both the baseline PLED process and PLED devices fabricated on integrated NB backplanes. The spectrophotometer was later incorporated into a semi-automated display characterization system , FPM 500, made by Westar Corporation (Figure 5.). This configuration will not only provide the basic information about the electro-optical performance and spectral distribution of emitted light, but can also measure the same characteristics at each pixel along both vertical and horizontal axes.

2.4 I-V Response Measurement Setup

The essential parameters of a PLED display, such as threshold voltage, rectification ratio, leakage current, efficacy and efficiency, can be directly or indirectly derived from I-V curve of the PLED device. We have assembled a computer-controlled setup for automatic I and V data acquisition via a LabView software program (provided by courtesy of Professor Yang Yang of UCLA). A programmable Keithley 2400 power supply (SourceMeter) and Keithley 2000 multimeter was acquired for the task.

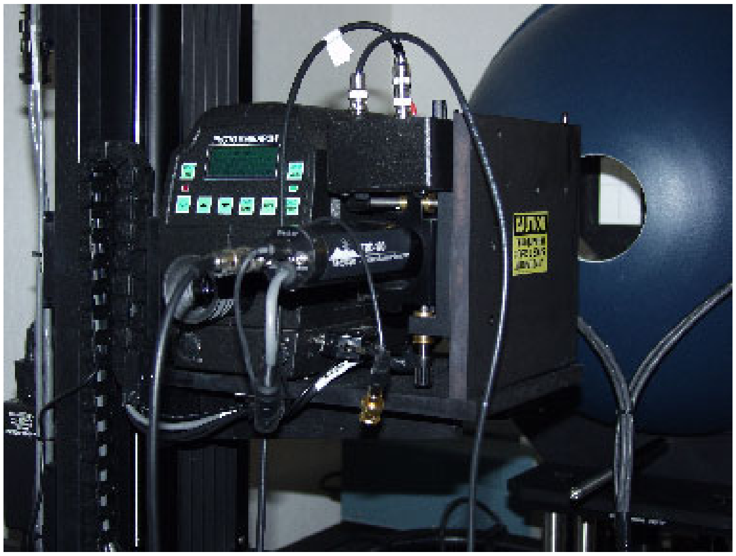


Figure 5. Setup for electro-optical characterization of PLED devices (displays). The photo shows a SpectraScan 705 next to a photomultiplier (TRD 100) for measurements of temporal media response. Both instruments are integral part of a Westar FPM 500 display measurement system.

Figure 6. Semi automated I-V curve measurement setup consisting of Keithley power supply, computer and software (courtesy of Professor Yang Yang, UCLA)

3. TEST VEHICLE 1

The purpose of the Test Vehicle 1 (TV-1) was to use an experimental substrate (vehicle) to establish the baseline PLED process on ITO/glass substrates. We adopted the process delineated in the Dow Chemical guide, which in turn affected the design of the TV-1 described below. TV-1 was also used for development of an alternative anode named “Grid Electrode” and for screening tests of barrier layers on plastic substrates (“lid test”). We also used a slight variant of the baseline process to produce an animated Alien logo to study the effects of incorporating an interlayer dielectric (ILD) in the PLED structure.

3.1 TV-1 Design

The layout of the device is shown in Figure 7. There are three 1 cm2 devices (coupons), and three “web” structures. The coupons were designed so that the active area of the PLED device would be the same (1 cm2) regardless of misalignment between anode and cathode.

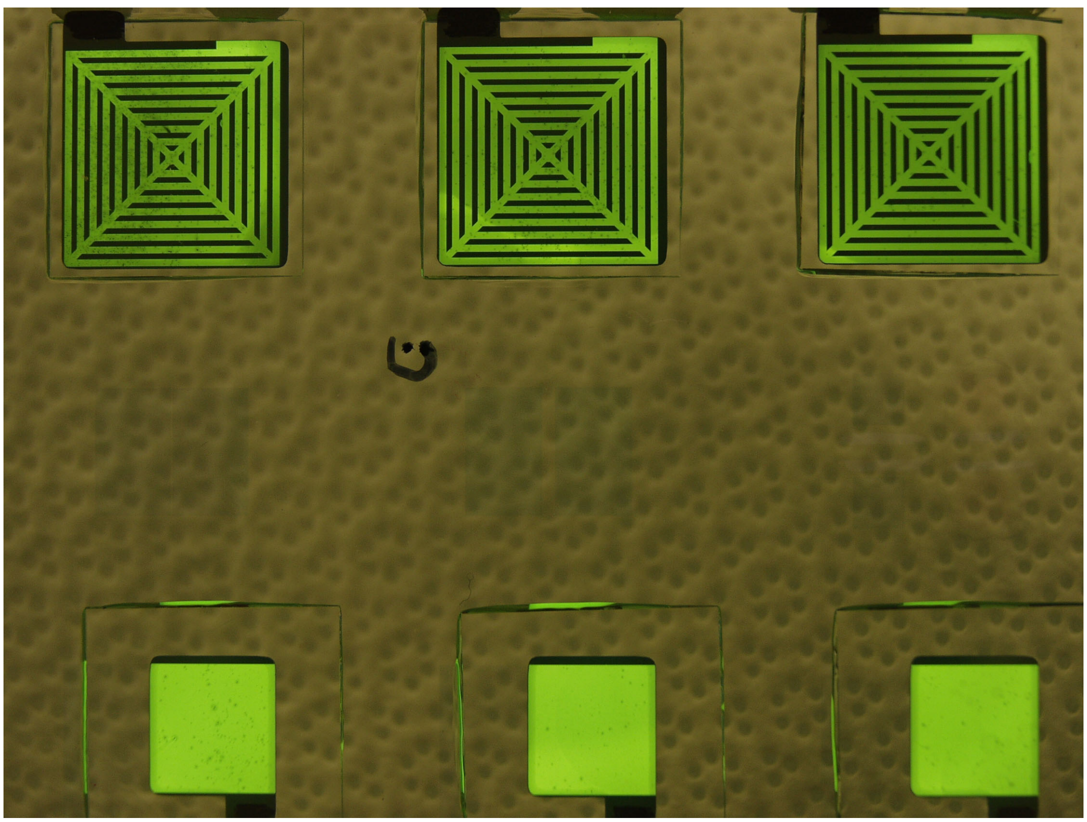


Figure 7. Layout of TV 1 test structures is shown by light emission.

The “web” structure was design for study of deterioration of the device due to diffusion of oxygen or water through the epoxy sealant (Figure 9). For these simple tests this encapsulation was adequate, but direct incorporation of the barrier layer into the structure itself is a goal of advanced structures. The “web” pattern, however, served us well when

the process development run into PEDOT/ITO wetting problems as described later in paragraph 8.3.2.2.

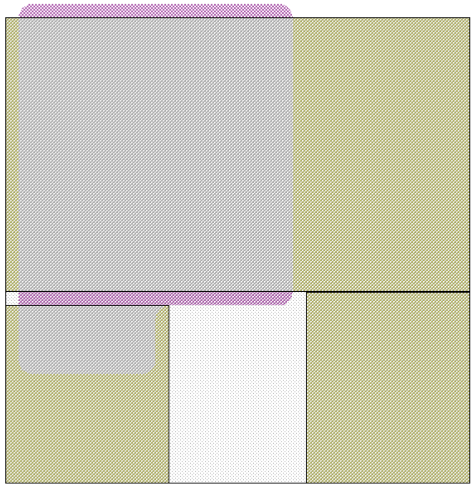
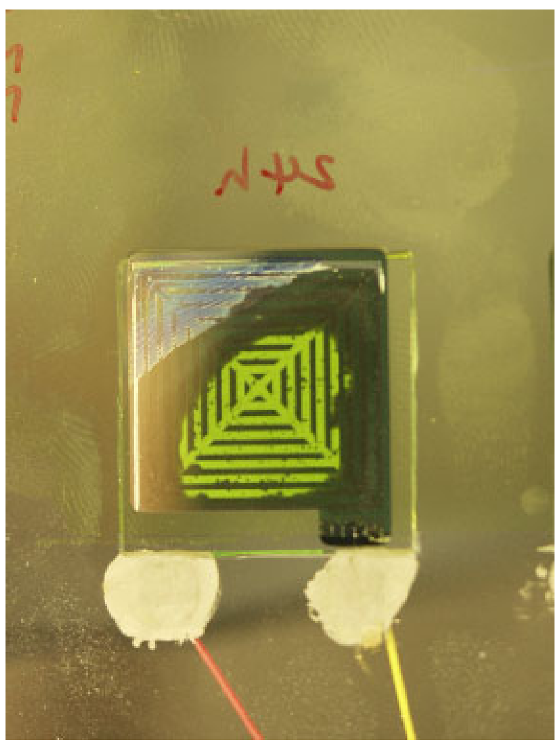


Figure 8. Design of anode/cathode overlap on the 1 cm2 device to be insensitive to possible mask misalignment.



into the active area of the device. An extremely bad case was chosen for illustration purposes.

3.2 Baseline Process

After several iterations, we established a Baseline Process to produce PLED devices on ITO/glass substrates. This Baseline Process provided acceptable performance, and served as a benchmark for evaluating other PLED devices under development. The Baseline Process is described in detail in Appendix A. In this section we will disclose the typical performance characteristics of our devices and compare them with data provided by Application Laboratory at Dow Chemical (Table 1.). We did not aim at PLED performance improvements beyond the level that was deemed satisfactory for demonstrating a successful integration of PLED structure with a NB back plane.

Table1. Performance comparison PLED Devices

In-house produced PLED devices by Baseline Process with performance data on devices prepared by Dow Chemical Application Lab

	Alien PLED Device*	Dow Chemical Appl. Lab*
Luminance (cd/m^2)	200 –300	300-500
Efficiency (cd/A)	2-3	3-5
Efficacy (lm/watt) @ 5V	1.5-2.0	~5.0
Time to half brightness	1 month @ 300cd/m^2	15 months @ 100 cd/m^2
Rectification Ratio (I_{fwd}/I_{rev}) @ ±7V	1,000 – 5,000	~ 5,000
Threshold Voltage (Vth)	2.0 V	1.8 – 2.5

* Using Dow Chemical Green B emitter (polymer)

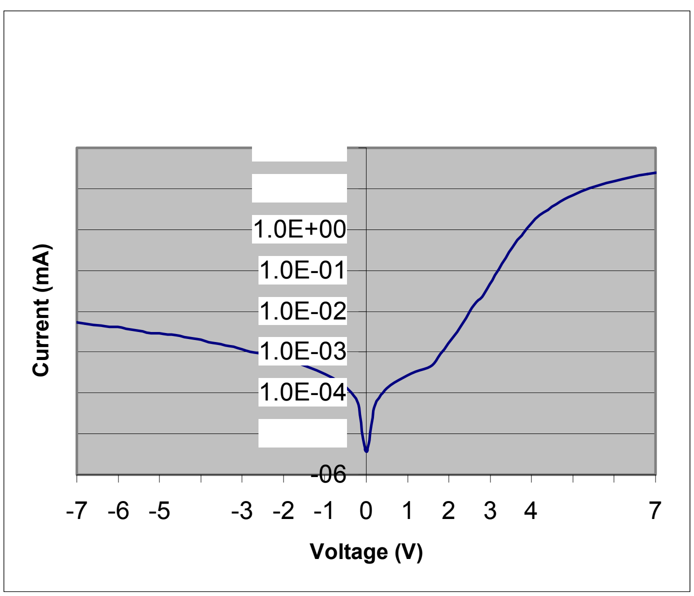


Figure 10. I-V curve of typical PLED device produced by Base-

A typical I-V curve is shown in Figure 10. We should note, that while on occasion we also worked with Red and Blue Emitters (Dow Chemical), for process optimization we used exclusively the Green B and/or Green K emitters.

3.3 Grid Electrode

We successfully used the TV-1 vehicle for the development of an alternative transparent anode that does not require ITO at all. The three basic functions of ITO (transparency, conductivity, work function) can be achieved by the combination of metallic grid (molybdenum) and a conductive polymer (PEDOT). We tested several combinations of grid line width and pitch with Bayer or Agfa PEDOT. The most successful was 10μm wide Mo lines with a pitch of 230μm combined with Bayer PEDOT. The transparency was 85%. The performance was sub par compared to devices with an ITO anode, exhibiting lower initial brightness and faster aging). An example of a device with a grid electrode is shown on Figure 11.

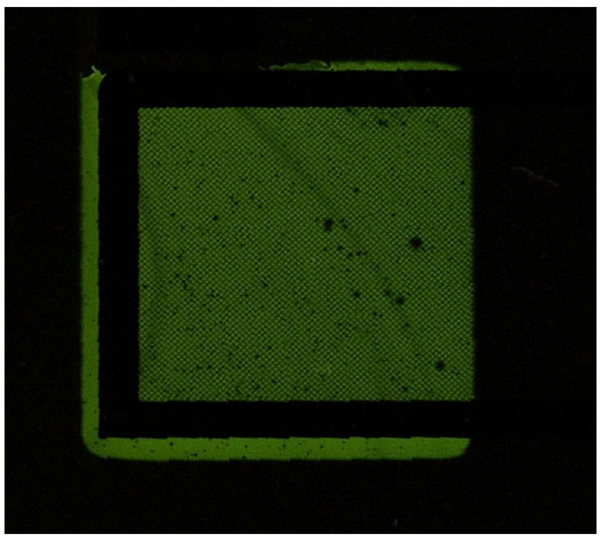


Figure 11. The visual appearance of a TV-1 device with a grid electrode after 160 hours of life test.

3.4 Logo Display

The original development of an animated Alien Logo (display glass and case with interface electronics) was performed in cooperation with professor Yang Yang (UCLA), and occurred before this DARPA Contract was awarded to Alien. Its main purpose was to demonstrate the capability of NB ICs to produce enough current to drive PLED device. We proved this capability by adopting a modular approach in which the Alien NB IC drivers were deployed on a separate substrate, and combined with a glass display produced at the UCLA PLED laboratory. However, we decided to produce similar devices under the DARPA program (i.e., designed our own mask set) for several reasons:

- to compare an in-house made devices with our "yardstick" from UCLA
- to verify we can incorporate an interlayer dielectric (ILD) into our PLED structure. The incorporation and patterning of such layer defines the shape of the Logo image. On the other hand, this layer is in direct contact with the most sensitive PLED materials, and the Logo display provides an opportunity to study the effects the presence of such layer has on the PLED device performance.
- We also grouped four displays on a 4"x4" glass substrate to optimize the uniformity of spun-on layers over the entire substrate area. The substrates were also used to practice display singulation.

Several iterations were needed to perfect the Logo Process, which is fully described in Appendix B. We perfected the spinning process of PEDOT and LEP solutions and achieved a high degree of uniformity (±10%), and improved the device lifetime from few weeks to several months. We also proved that a positive photoresist could be successfully incorporated into the PLED structure without significant detrimental effects on the device performance (Figure 12). Same photoresist was later used in our integration efforts as ILD on TV-2 segmented and matrix displays.

4. JADE: PLED SPECIFIC NANOBLOCK IC

The Jade is the code name used within Alien Technology to refer to the NanoBlock IC designed for direct drive of constant current PLED/OLED displays. The Jade NanoBlock IC (Figure 13.) is an 8 output, process insensitive current driver for PLED displays fabricated in a standard CMOS three metal process with 0.6 um minimum gate length transistor rules. It is intended primarily for direct drive applications, be it a dot matrix display or a segmented display. The Jade NB IC proves that it is possible to achieve process insensitive output current with a simple, static, scaling insensitive and compact compensation scheme.

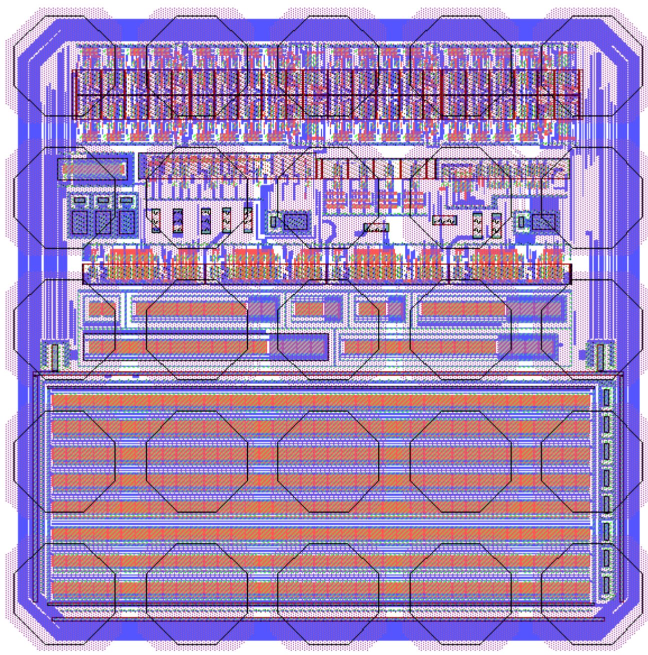


Figure 13. Layout of the Jade NanoBlock IC. The physical size

4.1 Advantages of NanoBlock ICs for PLED Displays

NanoBlock ICs are small, shaped die, typically made of crystalline silicon, with characteristic dimensions ranging from under 100 um to larger than 1 mm. These die are smaller than can be cost-effectively handled by pick-and-place machines, and Alien Technology Corporation's patented Fluidic Self Assembly (FSA) permits their placement on a rigid or flexible (plastic) substrate to within microns of accuracy. In addition, this placement is being performed at record rates on roll-to-roll processing equipment.

Silicon CMOS circuits are fabricated in some of the best yielding and controlled industrial processes ever developed. A highly competitive, global market place and ready access to foundries with modest non-recurring engineering (NRE) charges assure rapid turn

times for designs and aggressive pricing of wafers. Contrary to amorphous silicon or polysilicon technology, a technology that assembles CMOS silicon does not bring with it cost of ownership for an expensive fab facility. Rather, this cost is distributed amongst hundreds of customers with thousands of designs.

In addition, CMOS silicon has outstanding electronic properties and unparalleled circuit density. Not only are threshold voltages low and carrier mobilities high, but devices are highly reproducible, stable over time, well characterized and adequately predicted in simulations.

The down side of CMOS silicon, namely its high cost per unit area (5 ¢/mm^2 or more in a sub-micron process), can be more than recovered in circuit integration density for many applications. What FSA processes afford is not only the ability to rapidly and in parallel place large numbers of compact processors and drivers onto a substrate and to interconnect them, but also to radically alter the architecture and design of the silicon circuitry.

For example, standard CMOS die waste substantial area for bonding pads. This is particularly prominent in passive matrix (multiplexed) display drivers with their many output channels. By contrast, *NanoBlock ICs interconnection pads lie on top of the circuitry*. This is possible because interconnecting the NanoBlock ICs does not use wire bonding, but instead employs low-resolution lithography (another highly parallel process). The pad area is thus saved.

This approach does of course create a problem: reaching the pads at the center of the NanoBlock ICs (interior pads) requires either blocking perimeter pads, or a two metal backplane process, with its associated lower yield and higher cost. Addressing this issue, the second major architecture difference between NanoBlock IC based circuits and standard CMOS die is that *NanoBlock IC circuits are distributed*. They break a large monolithic die into smaller pieces so that many more of the interconnection pads are perimeter pads that are readily accessible. For display systems, distributed drivers have the advantage that the NanoBlock ICs can be pitch matched to the display along its edge, reducing the number of lines between the controller and the row & column drivers to a handful or so. This avoids extensive routing space for interconnect wiring, a point particularly critical for current driven display media such as PLEDs. In the context of multiplexed displays, a good way to think of NanoBlock ICs deployed by FSA is as follows: this architecture affords the pitch matched driver integration of polysilicon without its cost of ownership and inflexibility, and it affords the excellent drive capability and uniformity of silicon without having to pave the entire edge of the display with expensive silicon.

A third key change in circuit architecture is that *NanoBlock IC circuits can be scalable and modular*. Rather than re-designing silicon to drive larger format or complexity devices, one simply adds more NanoBlock ICs, which can be of the same kind as for smaller, lower complexity systems if properly designed. Similarly, different circuit designs, each with their characteristic shapes, can be assembled simultaneously. This strategy dramatically reduces silicon nonrecurring engineering (NRE) costs.

4.2 Compensation of Silicon Fabrication Process Variation in Jade

The current drivers in Jade are designed to be insensitive to fab process variations. As such, they address a potentially fatal drawback of current driver NanoBlock ICs assembled by FSA. Namely, the NanoBlock ICs assembled side by side in a display likely originate in different portions on the same wafer, on different wafers of the same lot, or even on wafers of different lots. The variability of silicon material parameters across wafers and lots is far worse than within a small area of a given wafer and is often of the same magnitude as the across-panel variability of competing technologies, for instance low temperature polysilicon.

Digital voltage drivers usually suffer less from process variations. While their drive capability may vary, the output voltages are usually dictated by the supply rails and remain unaffected, unless the output voltage levels are derived from a lower supply voltage by a multiplication process. But current drivers are hit hard: two silicon transistor parameters governing the transistor output current, namely the threshold voltage VT and the transconductance parameter k´, change substantially from lot to lot. These parameters impact the transistor saturation current as follows:

$$I_{SAT} = -\frac{W}{2L} k'\left(V_G - V_S - V_T\right)^2$$

For example, the transconductance parameter is proportional to gate capacitance density (*i.e.*, inversely proportional to gate oxide thickness), which is specified in many fab processes to vary by as much as ± 10%. This alone would give rise to an unacceptably large current variation.

As a rule of thumb, acceptability of brightness non-uniformity depends on the type of non-uniformity. The human eye tolerates pixel-to-pixel brightness variation of about 5%, but only 2% - 3% line-to-line non-uniformity and only about 1% - 2% non-uniformity block-to-block. With NanoBlock ICs driving blocks of pixels, output current uniformity requirements are stringent.

A number of compensation schemes have been tried. Some schemes compensate for threshold voltage variations only, while others attempt a dynamic calibration method. This latter approach uses the rate of discharge of a capacitor through a transistor identical to those in the current sources to monitor transistor output current and null out process variability. None of these methods are capable of the required performance we need, as they either address variation of only one of two important parameters, or employ capacitors whose values are themselves afflicted with at least the same variability as the transistor parameters.

In the Jade NanoBlock IC, we took a novel approach. The compensation circuit we invented uses an overcompensation scheme that measures the threshold voltage alone, and then compensates at once for both the threshold voltage and transconductance parameter

variations. The circuit is compact and static, not dynamic. It has the potential for very low power consumption and for supply voltage insensitivity, although both features were not designed into Jade to expedite fabrication. Only one compensation circuit is required for all output current sources on board the NanoBlock IC.

Approximately 60% of the area of a NanoBlock IC is occupied by the eight output current drivers, which are sized much larger than minimum dimensions to assure device matching in the absence of hard foundry matching parameters foundry. In the interest of time and to conserve silicon real estate, not all layout techniques for device matching were implemented.

4.3 Circuit Architecture

The Jade NanoBlock IC circuit architecture is described in the block diagram of Figure 14. A description of the individual block functions follows below. The 5 x 5 NanoBlock IC pad frame is shown in Figure 15 with pad functional assignments, and Figure 16 gives a typical inter-connection scheme for two Jade NanoBlock ICs. A direct drive matrix display implementation can be seen in Figure 17. Note that contrary to both passive matrix and most active matrix displays systems, direct drive does not entail crossing signal lines, thereby reducing cross-talk and eliminates opportunity for row-column shorts.

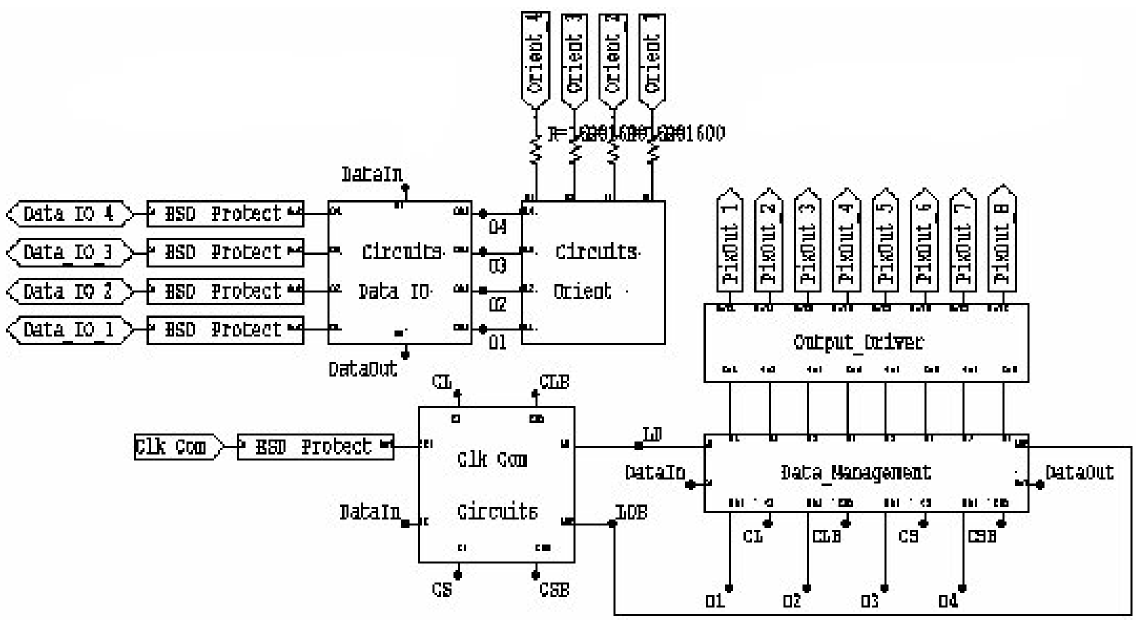


Figure 14. Jade NanoBlock IC circuit architecture

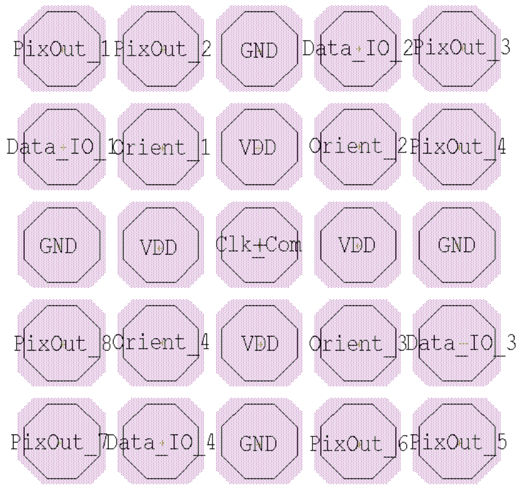


Figure 15. Jade NanoBlock IC pad frame with pad functional assignments

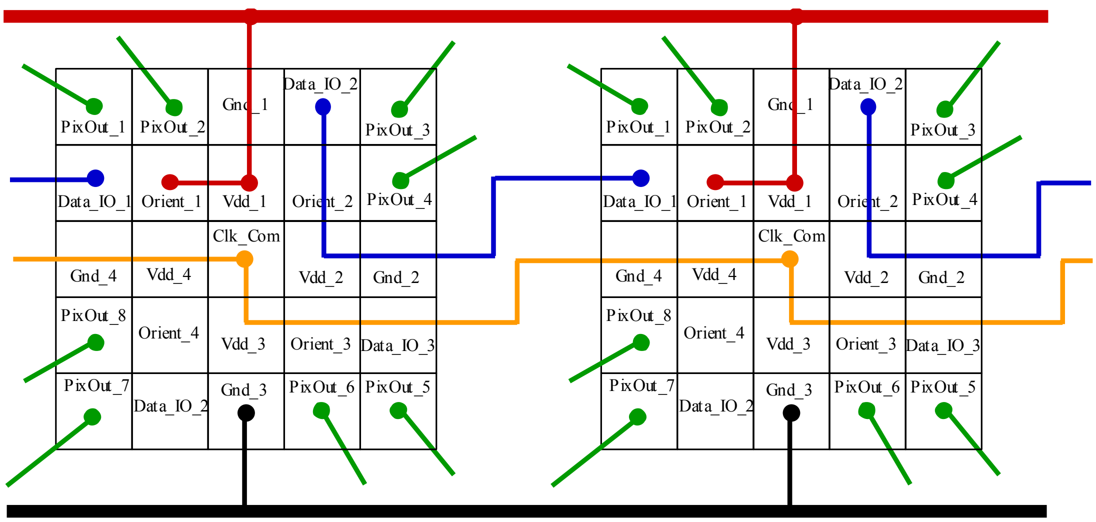


Figure 16. Typical inter-connection scheme for two Jade NanoBlock ICs

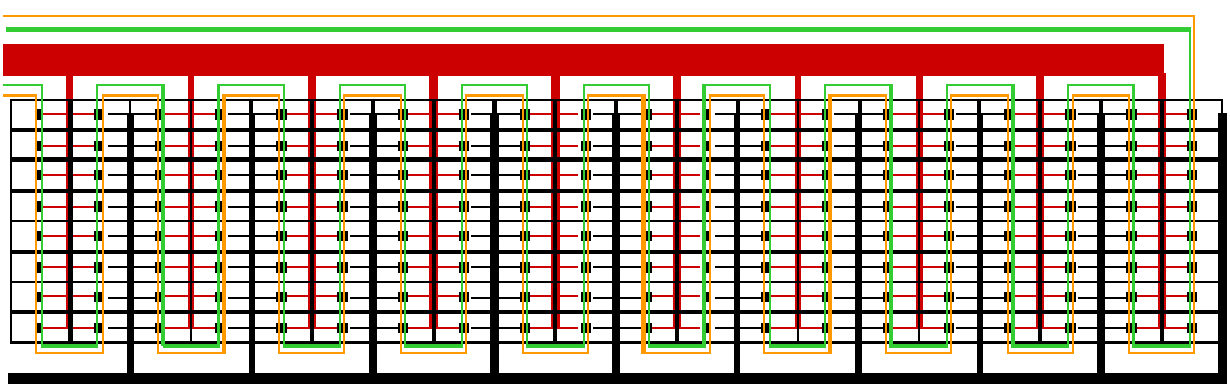


Figure 17. Direct Drive matrix display using NanoBlock IC

4.4 Data Management

The data management section of Jade consists largely of a 32 stage static shift register to manage four bits of digital gray scale (16 levels) for each of the eight output channels. If two or more NanoBlock ICs are connected in a serial string, the data are shifted into and out of each NanoBlock IC shift register and are then moved into the next NanoBlock IC.

Commands and clock pulses are riding on a separate common Clock/Command line and are encoded as long and short pulses, respectively. Gray scale is implemented in the time domain by successively applying the four bits associated with each output channel for time intervals that vary by a factor of two from interval to interval. Data are loaded during the longest time interval available (most significant bit) and then successively shifted using the long Command pulses (Fig. 18). Note that in this scheme, all data for the entire chain of NanoBlock ICs (if there is one) has to be loaded in this longest time interval, which is approximately half the refresh period. With modifications, the same scheme can also be applied to passive matrix drive, although it is not necessary to load all data in the longest time interval.

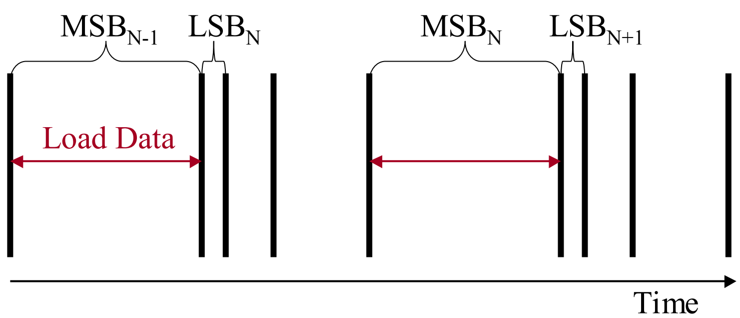


Figure 18. Implementation of time domain digital to analog conversion

4.5 Orient Circuit

The square shape of the NanoBlock IC allows it to drop into a receptor site in four distinct orientations, which need to result in the same functional performance. To retain a maximum level of compatibility with Alien's existing Zircon design, the same 5 x 5 pad frame was retained. Since Jade is a low voltage (5V) design, NanoBlock IC orientation can be easily determined by tying one of the four equivalent orient pads to the power supply. The Orient circuitry itself was very different. Each Orient pad is connected to an Orient circuit. The four Orient circuits are configured into a winner-takes-all system. In this system, each Orient circuit tries to drive all other Orient pads to ground. The one pad tied to VDD cannot go to ground and therefore wins the competition. The circuit consumes no power in steady state.

The Orient circuit assigns Data In and Data Out pads and routes the data to the appropriate outputs. There are four equivalent Data I/O pads that are each driven by a tri-state driver. If an Orient pad is tied to the power supply line, it assigns the Data I/O pad next to

it the Data Input and the nearest clockwise Data I/O pad the Data Output. The remaining two Data I/O pads are left floating (disconnected).

4.6 Clock and Command Circuit

The clock and command circuit determines whether an incoming pulse is a long (command) or short (clock) pulse. Both pulses generate a set of complementary clocks on their trailing edge. In addition, detection of a long pulse latches the contents of every fourth data register into the eight output current drivers.

4.7 ESD Protection Circuits

The ESD protection circuits consist of an n-well resistor followed by a reverse diode to ground and a PNP bipolar junction transistor. Due to space constraints, they are rather unsystematically distributed within the layout, and Orient pads are only protected by an n-well resistor. As a general rule, each Data I/O pad, Orient pad and the Clock/Command pad must be ESD protected. Reverse diodes between power and ground as well as between pixel current outputs and ground complete the ESD structures.

4.8 Results

4.8.1 Output Current Uniformity

In cooperation with the foundry, die from a total of six different lots were evaluated. To this end, all 1028 current outputs of a 128 NanoBlock IC test structure surrounding the stepper field (proxy testing) were analyzed for average, maximum and minimum output current as well as standard deviation. On each wafer polled, three such test structures were analyzed, on three wafers per lot.

Our finding is that amongst these six lots run at the foundry over the duration of half a year, overall output current variation was ± 4%. The variability within a single NanoBlock IC was better than ± 1%, and the lot averages varied by no more than ± 1.5%. The most surprising finding was that variations from one NanoBlock IC to its next neighbor could be as high as 2%. This points to a matching problem rather than a basic problem with the compensation philosophy. Neither threshold voltages nor doping densities should vary so rapidly from site to site, and the analysis of Scribe Line Monitor results supports this contention.

The performance of Jade is almost identical to that of commercially sold OLED drivers (Claire Micronix MXED102, current variability ± 2% ± 1.5 uA intra-die, ± 1% inter-die). Given that the circuit was implemented in a foundry that does only 10% of its business in mixed signal, we view the demonstration of the compensation scheme as successful with room for substantial (at least factor of 2) improvement.

Stepper fields are sort tested at the foundry, and only stepper fields in which all outputs in the 128 NanoBlock IC ring test structure report currents within ± 3% of a fixed average value are released as NanoBlock ICs. Our NanoBlock IC data sheet therefore references an output current uniformity of ± 3%.

4.8.1.1 ESD Sensitivity

The area afforded to ESD protection is only a fraction of the required area to achieve 4 kV protection. It is therefore not surprising that the NanoBlock IC fails ESD tests between 100V and 200V. Future improvements could include rounded geometries for the diode and *pnp* bipolar junction transistor, complete protection of all sensitive pads, better distribution with proximity to pads, and larger area which can be afforded by a change in NanoBlock IC geometry. With rotation asymmetric shapes, no functionality is lost, and the number of ESD sensitive pads (Clock/Command, Orient, Data I/O) is reduced from nine in the case of a square NanoBlock IC to three in the case of a rotation asymmetric NanoBlock IC.

5. TEST VEHICLE 2

After establishing the Baseline Process utilizing TV-1, the next step was to proceed with process integration that would successfully demonstrate high quality PLED displays on top of the NB backplane with embedded NanoBlock ICs. For that very purpose we designed the Test Vehicle 2 (TV-2).

5.1 Initial TV-2 Process

The process we originally designed for a PLED specific backplane intentionally mimicked the Standard Manufacturing Process in place at Alien at that time (Appendix D). This process was designed to produce small reflective PDLC displays (Figure 19). Several modifications to this design were necessary for PLED displays. The incorporation of a transparent anode allowed the light generated within the LEP to escape towards the viewer through the substrate, and introduction of interlayer dielectric (ILD) prevented shorts between Al traces and metallic cathode.

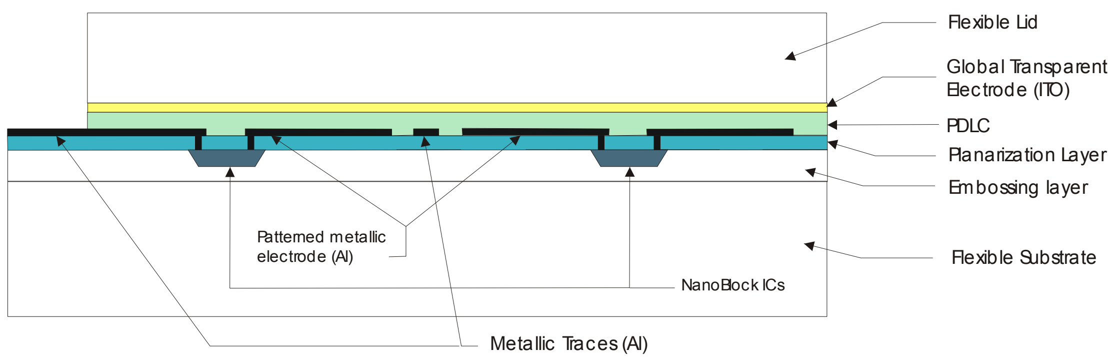


Figure 19. Structure of reflective PDLC display incorporating NanoBlock ICs

After the incorporation of ITO and an ILD, the integrated NB backplane for PLED displays is shown in Figure 20. The process initially proposed for this structure is described in detail in Appendix E, and was used as a foundation for the design of TV-2 backplane as described below.

5.2 TV2 Description

TV2 is a set of backplane designs intended as process development vehicles for polymer LED (PLED) fabrication processes with integrated Jade NanoBlock IC PLED current drivers. It also serves as Alien's first PLED displays with integrated NanoBlock IC drivers.

TV2 is fabricated on 4” x 4” x 1.1 mm glass sheets. The surface layer that the PLED device is built on is a polymer layer. This approach has a number of advantages. The underlying glass substrate is more dimensionally stable and easier to fabricate on than on standalone plastic film. With the top layer being a polymer, the most important challenges arising in PLED fabrication on plastic can still be studied: lifetime of the devices, chemical compatibility, and fabrication on a rougher, softer surface than is the case on glass. Indeed, the plastic substrate is, to first approximation, merely a carrier with receptor sites for NanoBlock ICs. In TV2, the receptor sites are cast with a silicon mold wafer into a polymer film spread onto the glass.

The backplane comprises two types of displays (a five digit, eight segment numeric display as encountered in smart cards, and a 16 x 24 direct driven matrix array), test structures, process monitors and alignment marks. These will be described separately below.

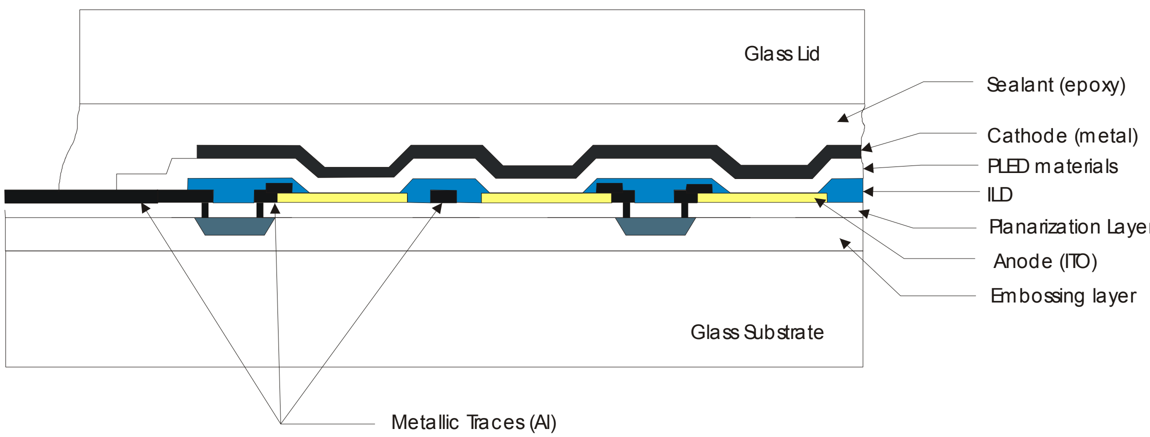


Figure 20. Structure of PLED display with ITO anode replacing the original aluminum electrode and additional layer of ILD. This structure served as basis for the

5.3 Process Flow

Here we describe the basic process flow and features of TV2 Rev A. TV2 Rev B through Rev D are then reviewed in terms of how their process flow and layouts differ from Rev A.

The major process steps and associated [mask layers] are as follows:

1) Form NanoBlock IC receptor sites [SUBSTRTATE ETCH].
2) Place NanoBlock ICs by Fluidic Self Assembly [FSA].
3) Planarize with polymer overcoat. [PLANARIZE]
4) Deposit, pattern PLED anodes (Indium Tin Oxide, ITO) [ITO]
5) Pattern vias to NanoBlock ICs [DISPLAY VIA1]
6) Deposit, pattern interconnect metal (aluminum) [DISPLAYMETAL1]
7) Deposit, pattern interlayer dielectric (ILD) [DISPLAYVIA2]
8) Spin coat hole transport layer [HTL, PEDOT]
9) Spin coat Light Emitting Polymer [LEP]
10) Evaporate calcium (10 nm) / aluminum PLED cathode through shadow mask, [CATHODE METAL]
11) Encapsulate

More detailed information is given in the Appendix E.

5.4 Backplane Layout

Figure 21 shows the entire TV2 backplane layout. The specific elements are discussed below.

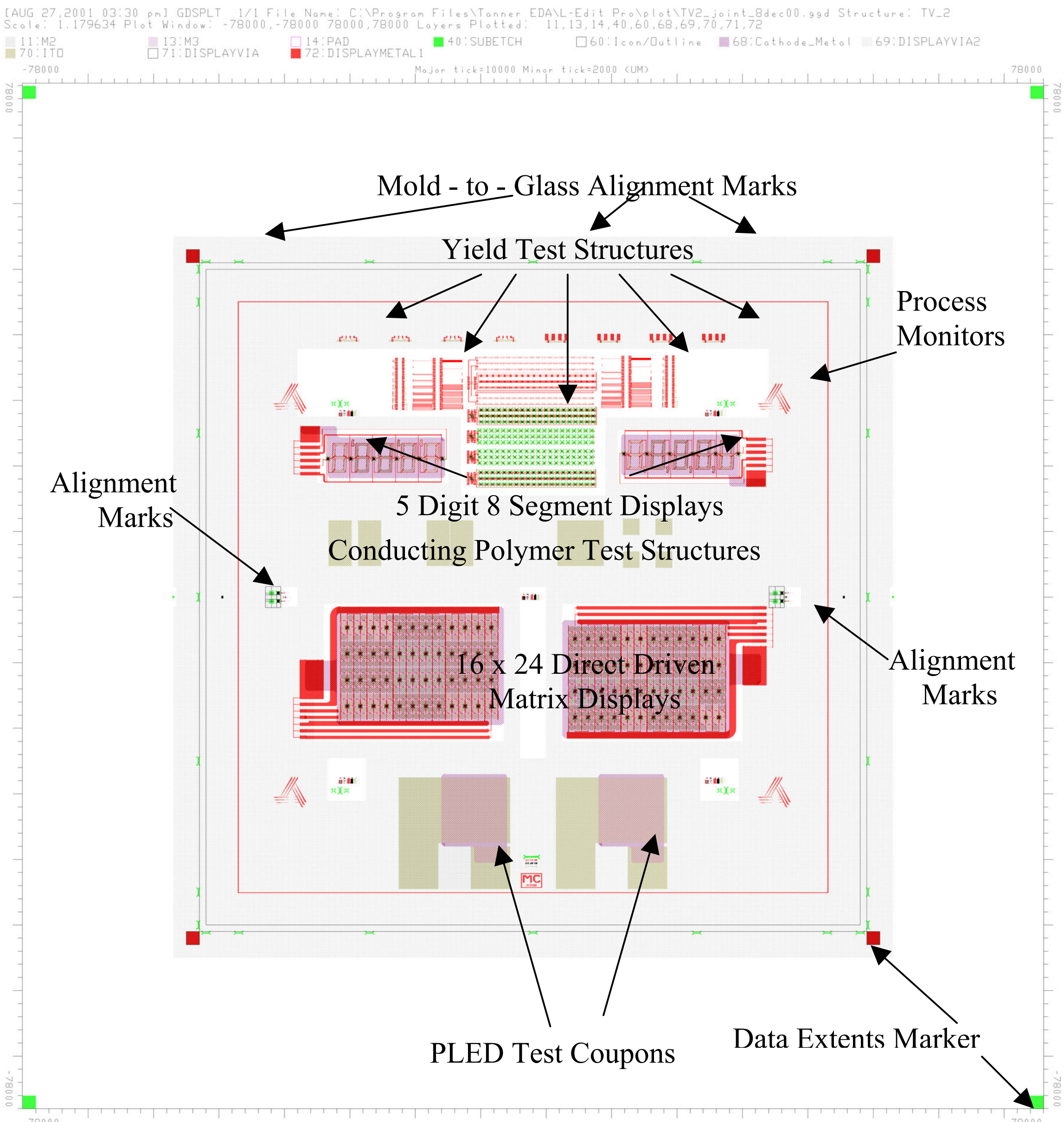


Figure 21. TV2 Backplane Layout

5.5 Alignment Marks

The alignment marks are shown in Figure 22. They are located on right and left side of mask. The pattern is copied, not mirrored.

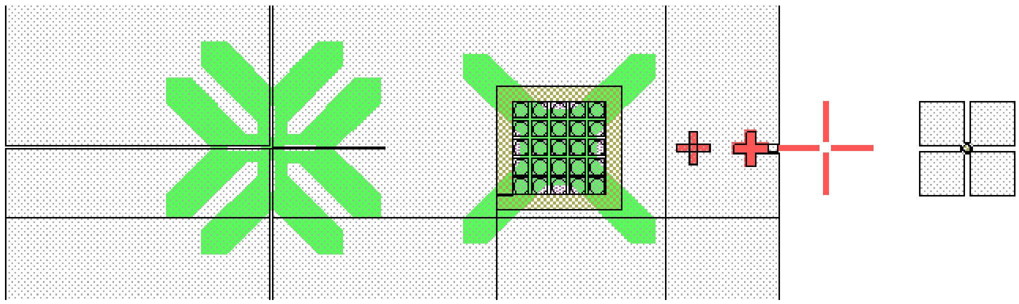


Figure 22. Alignment marks on TV-2

Alignment marks are, from left to right:

- DISPLAYVIA1, ITO and DISPLAYVIA2 alignment to cross cast into the substrate. Alignment employs the following features on the respective masks: a cross drawn in the ITO layer (bright field mask), inverse crosses drawn in DISPLAYVIA1 and DISPLAYVIA2 layers (dark field masks). These marks are currently not being used.
- ITO, DISPLAYVIA1 and DISPLAYVIA2 alignment to FSA'ed NanoBlock IC. Framed chrome grids on the ITO, DISPLAYVIA1 and DISPLAYVIA2 masks is aligned to the 5 x 5 NanoBlock IC Metal 3 pad array.
- Cross to align the DISPLAYMETAL1 mask to a slightly larger cross patterned into the DISPLAYVIA1 layer.
- Cross to align the DISPLAYVIA2 mask to a slightly larger cross patterned into the DISPLAYMETAL1 layer.
- DISPLAYMETAL1 crosshairs for alignment to DISPLAYVIA1 via (20 um nominal, 28 um after patterning).
- DISPLAYVIA2 chrome crosshairs aligning to an ITO circle patterned onto the substrate.

5.6 Process Monitors

Process monitors are located in each of the four corners. The patterns are copied, not mirrored.

5.7 Five Digit, Eight Segment Displays

Each backplane contains two five-digit eight-segment numeric displays (Figures 24 and 25). This layout is a simplified version of the Alien's smart card display, stripped of extraneous features associated with fabrication on roll-to-roll equipment and product test (e.g., probe pads and cut marks are removed).

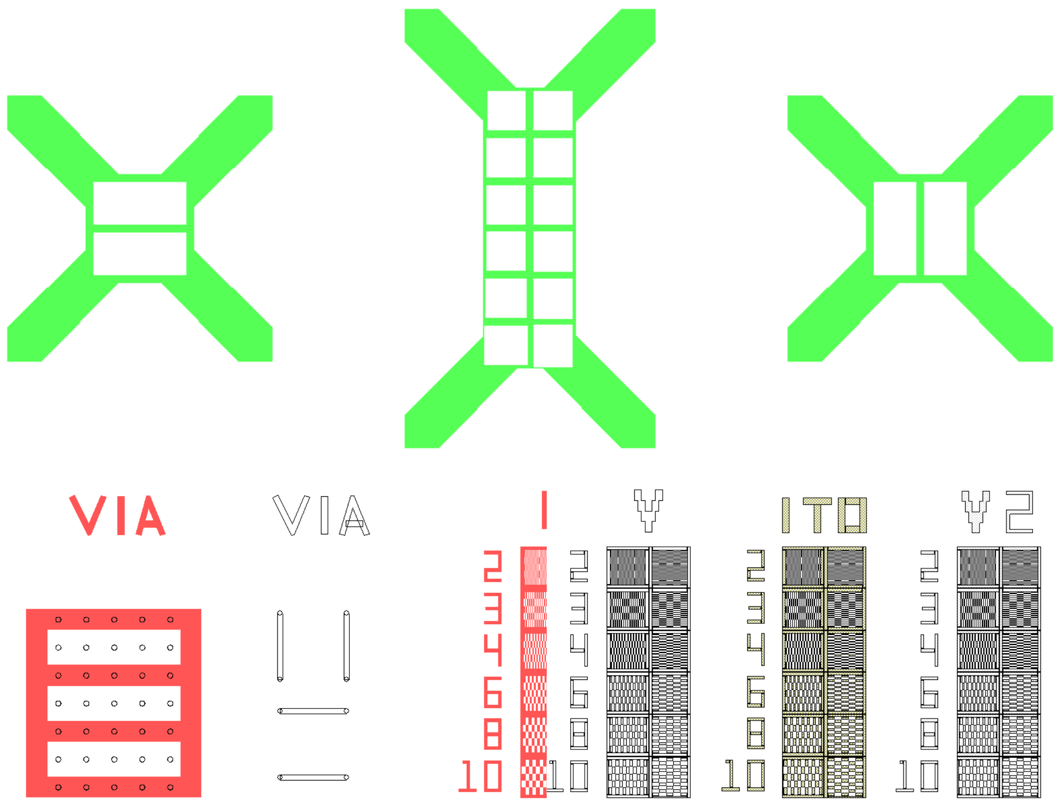


Figure 23. Top: Horizontal and vertical line-space resolution patterns (center) flanke tor hole etch monitors. Bottom: DISPLAYVIA1 ("VIA") monitors (left) as well as DISPLAYMETAL1 ("M"), DISPLAY , ITO ("ITO") and DISPLAYVIA2 ("V2") vertical and horizontal line space resolution patterns.

Design rules area minimum line-space width was 50 um-50 um in the display area.

To prevent voltage drop across the ITO segments (ITO on polymer layers typically has high resistivity), all segments were surrounded along their perimeters with a 20 um wide DISPLAYMETAL1 loop on the inside, abutting the outside edge of the segments.

All segments (except for the comma segment) possess equal area within +/- 1%, so that equal currents as generated by the Jade NanoBlock IC result in equal brightness. The

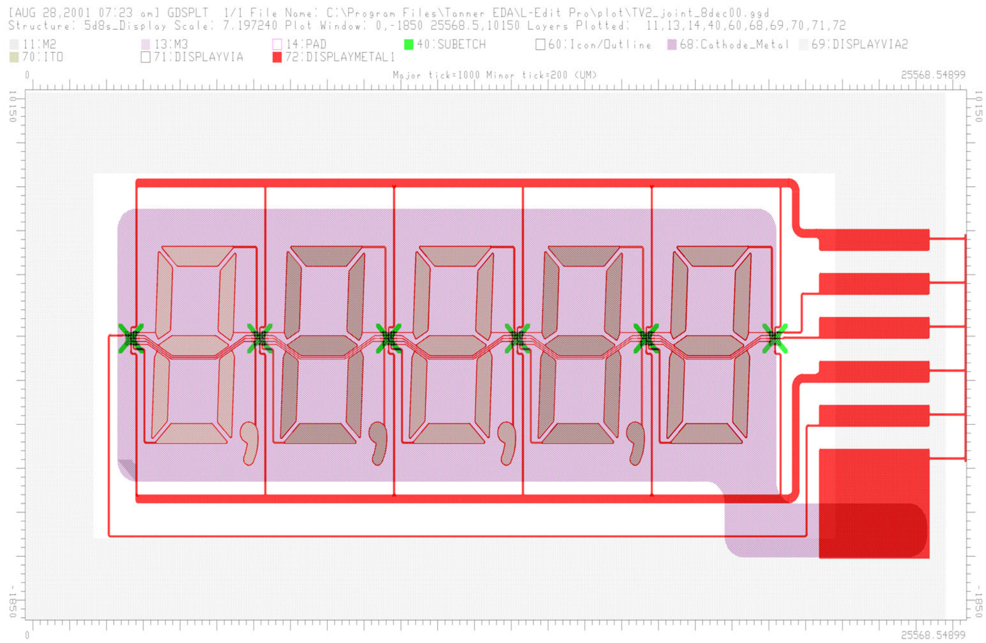


Figure 24. Five digit, eight segment display. The non-uniform shading of the digits is an artifact.

brighter appearance of the comma is acceptable in a demo device. In addition, the gray scale capability of the Jade NanoBlock IC can be used to equalize the brightness if desired.

The corners on all DISPLAYMETAL1 lines are rounded except in some test structures, with the inside (outside) corner radius 50% (150%) of the line width. This feature allows portability to flexible substrates where stresses could cause lines with sharp turns to break.

Openings are patterned into the DISPLAYVIA2 layer over the portions of the segments intended as ITO pixel anodes and over the DISPLAYMETAL1 I/O pads so that signals can be brought in. DISPLAYVIA2 overreaches the DISPLAYMETAL1 contact loops by 10 um. The I/O pads are shorted together by a shorting bar to avoid damage by ESD before singulation. DISPLAYVIA2 is also removed along the perimeter of each display for better encapsulation.

5.8 16 x 24 Matrix Displays

Each backplane contains two 16 x 24 matrix displays with octagonal pixels of 1 mm pitch. The pixels are not surrounded along the perimeter with a DISPLAYMETAL1 loop, but contacted only along one of eight edges. Fill factor is 60%.

Design rules are largely 20 um / 20 um lines & spaces, since most of the area is viewing and fill factor sensitive. Supply lines are 100 um wide to accommodate larger supply currents without excessive voltage drop along the line. The corners on all DISPLAYMETAL1 lines are rounded, with the inside corner radius 50% of line width and the outside corner radius 150% of line width.

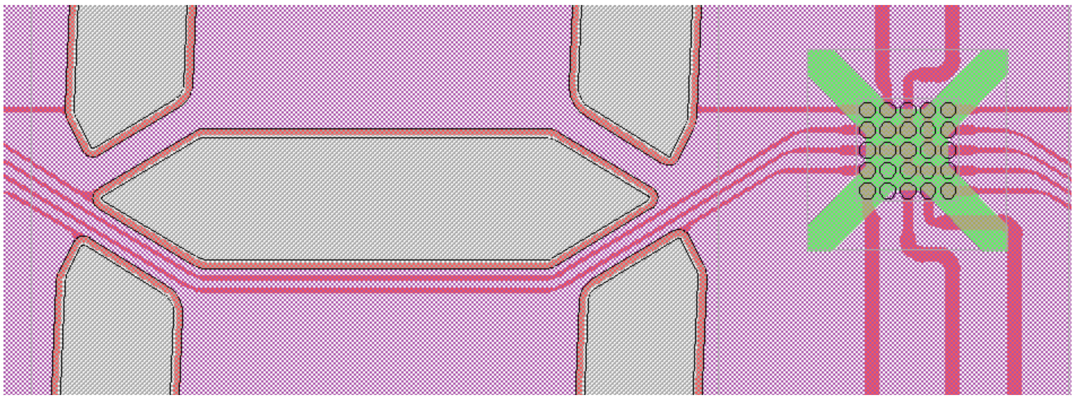


Figure 25. Pixel segments with DISPLAYMETAL1 contact loop, signal wiring between NanoBlock ICs.

DISPLAYVIA2 is patterned over the parts of the segments intended as ITO pixel anodes and over the DISPLAYMETAL1 contact pads so that signals can be brought in. Patterning over the ITO pixel anodes is such that DISPLAYVIA2 overlaps the aluminum contact straps by 10 um. Elsewhere the opening into DISPLAYVIA2 abuts to the outside edge of the ITO pixel anodes.

The I/O pads are shorted together by a shorting bar to avoid damage by ESD before singulation.

The pixel brightness is expected to be virtually identical to the 5 digit 8 segment display, as the opening into DISPLAYVIA2 differs by only a few percent from the segment area .

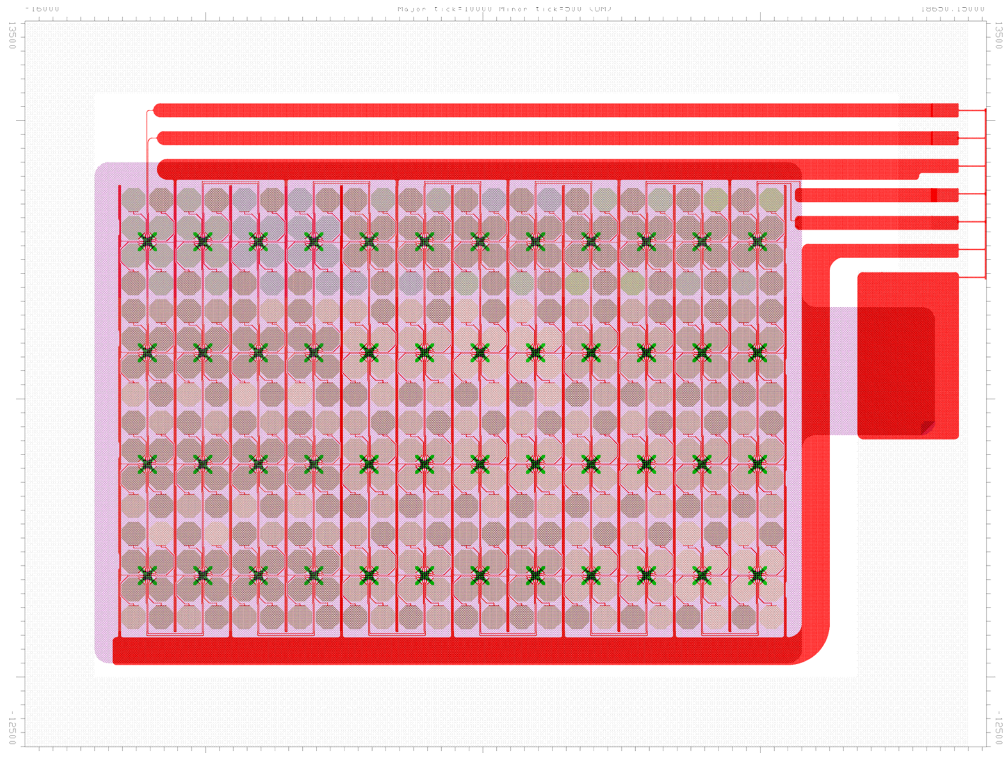


Figure 26. 16 x 24 Matrix Display. The non-uniform shading of the pixels is an artifact.

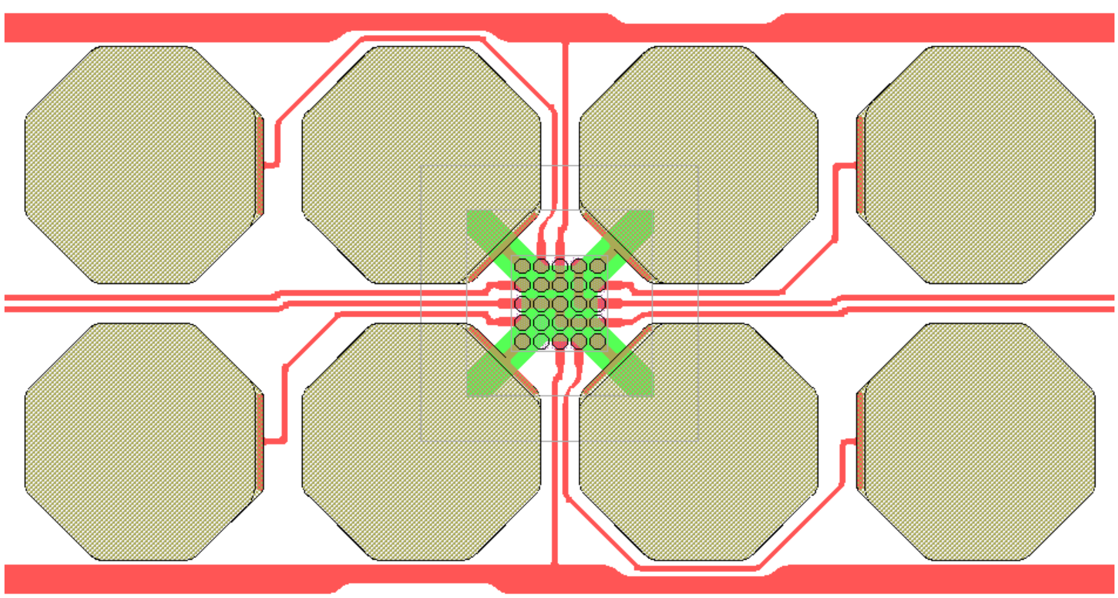


Figure 27. Eight Pixel Repeated Block Layout in 16 x 24 Matrix Display with NanoBlock IC

5.9 NanoBlock IC Test Structures

The following test structures are located at the top and center of the backplane.

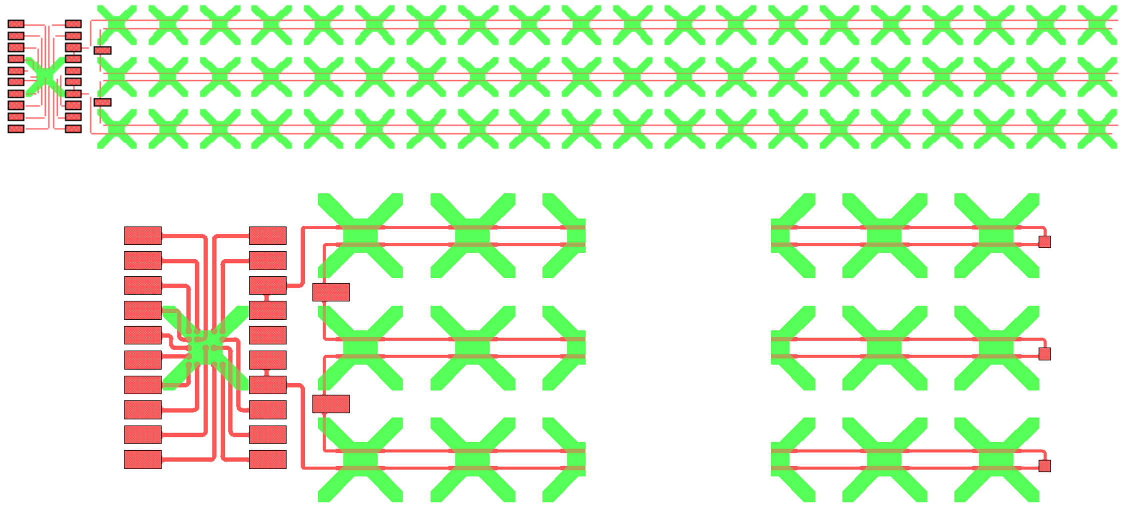


Figure 28. Line continuity over NanoBlock IC test structure. Three *x* twenty NanoBlock IC array to test DISPLAYMETAL1 line continuity over NanoBlock ICs. The layout of the serpentine wire is the same as the one running over the field to assess yield degradation due to NanoBlock ICs. Also, single NanoBlock IC test

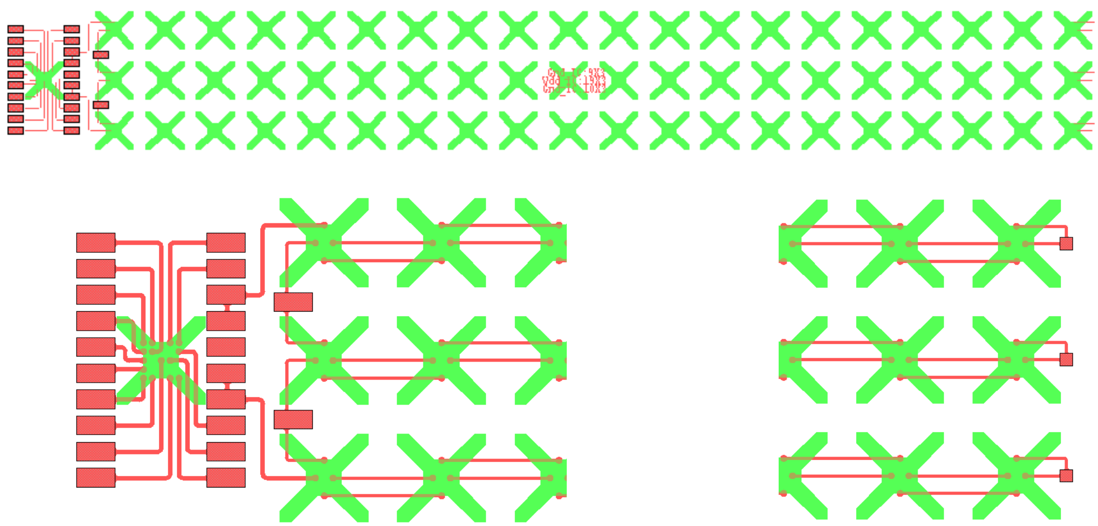


Figure 29. Via continuity and resistance into and out of NanoBlock IC test structure.3 x 20 NanoBlock IC array for test of DV1 via continuity into and back out of NanoBlock ICs and for average via resistance measurements. Also, single NanoBlock IC test structure

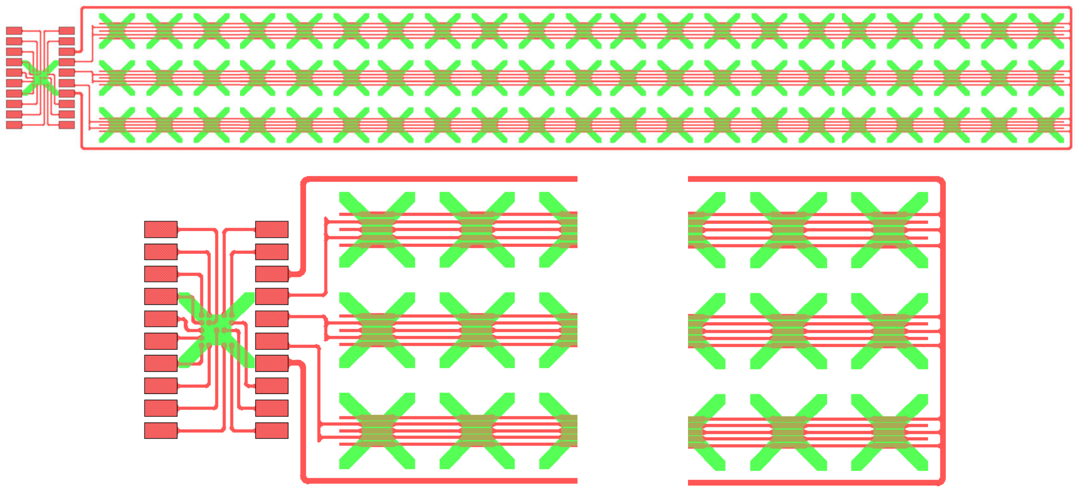


Figure 30. Space continuity over NanoBlock IC test structure Three times twenty NanoBlock IC array to test DISPLAYMETAL1 space continuity over NanoBlock ICs. The layout of the wiring structure is the same as the one running over the field to assess yield degradation due to NanoBlock IC presence. Also, single NanoBlock IC test structure. Three spaces are evaluated: 20 um, 14 um and 10 um.

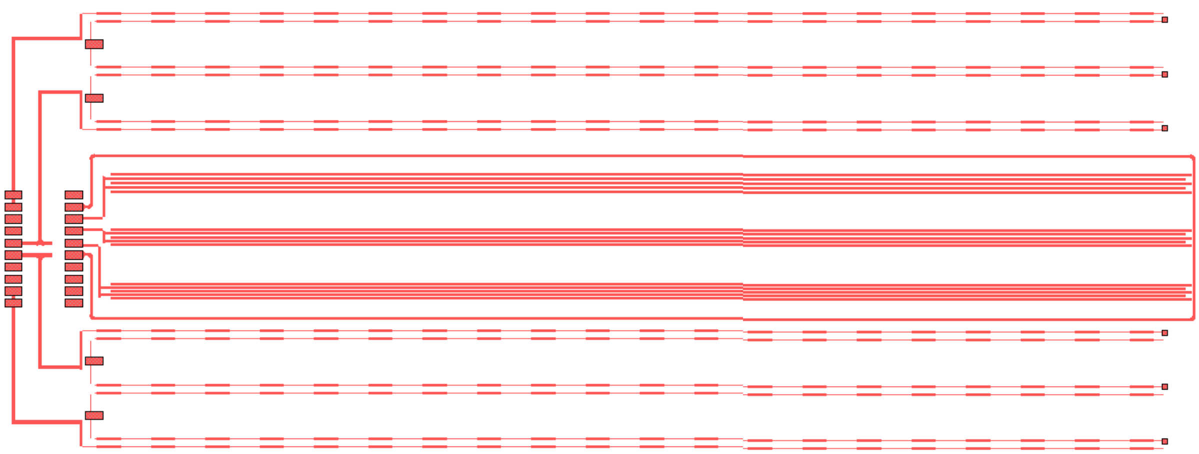


Figure 31. Line and space continuity over Field test structure. The DISPLAY-METAL1 wiring over the field is identical to the line continuity and the space continuity test structures running over NanoBlock ICs.

In the line continuity structures, lines are 20 um wide between NanoBlock ICs and 30 um wide over NanoBlock ICs, as in displays. Spaces over NanoBlock ICs are 107 um so shorted lines do not mask line continuity. In the space continuity test structure, the case is opposite: spaces over NanoBlock ICs are 20/14/10 um, and lines over NanoBlock ICs are 50 um wide, so that broken lines do not mask space continuity. Lines are also narrower

between NanoBlock ICs so test results are dominated by space yield over NanoBlock ICs, not over the field.

5.10 DISPLAYMETAL1

Serpentine lines are used as a line continuity test. Hence, the spaces are larger to make sure space continuity yield does not mask line continuity. Combs are used as a space continuity test. As such, the lines are wider to make sure line continuity yield does not mask space continuity.

Figure 32. DISPLAYMETAL 1 Serpentine (left) and comb (right) test structures. This structure allows design rule validation and DISPLAYMETAL1 thickness monitoring.

Display Metal 1 Serpentine Structures:

Serpentine Structure #	1	2	3	4	5	6	7	8
Line width [um]	6	8	10	14	20	25	30	50
Line Space [um]	8	10	12	16	22	27	35	55

Display Metal 1 Comb Structures:

Comb Structure #	1	2	3	4	5	6	7	8
Line width [um]	8	10	12	16	22	27	35	55
Line Space [um]	6	8	10	14	20	25	30	50

5.11 ITO Test Structures

Following are test structures used to monitor ITO film properties.

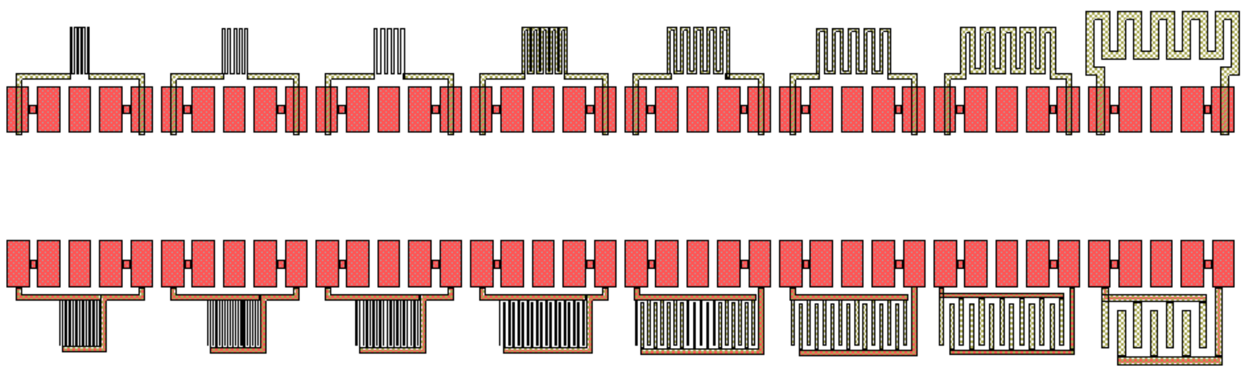
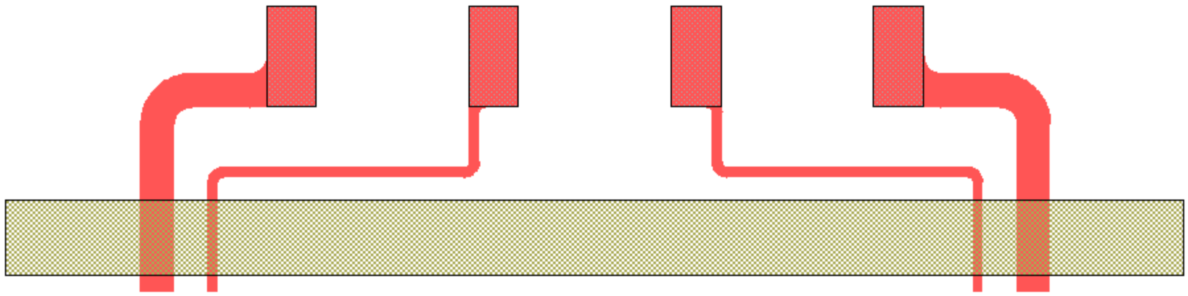


Figure 33. Comb and serpentine test structures for ITO, same idea as for DISPLAYMETAL1. Due to the much higher sheet resistivity of ITO (50-100 W/ð), the structures are held much shorter. Feature sizes are the same as in the DISPLAY-METAL1 comb and serpentine structures are held much shorter. Feature sizes are the same as in the DISPLAYMETAL1 comb and serpentine structures.



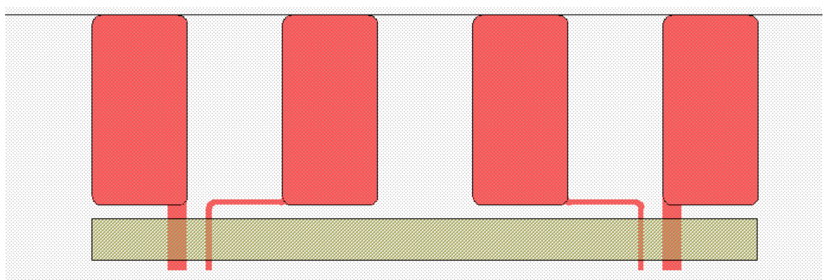


Figure 34. Two four-point probe structures to measure ITO sheet resistance and provide an estimate of ITO/DISPLAYMETAL1 contact resistance. The different probe pads (1 mm pitch and 600 um pitch) were chosen to allow automated (every third of 10 probes spaces 200 um apart) and hand probing and were separated as widely as possible to screen the effect of conducting polymer bridging electrodes.

5.12 Conducting Polymer Test Structures

The conductivity of polymer layers can be affected by processing. The coarse assessment of the state of either HTL or LEP can be made by measuring conductivity of the polymeric layers over known geometry of a gap between two ITO pads. These structures are very similar to those successfully used in TV-1.

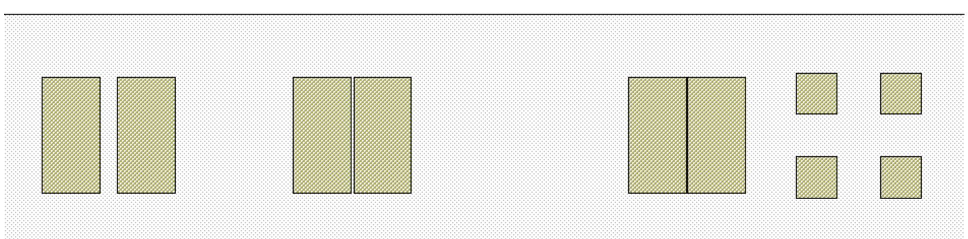


Figure 35. Test structures have gaps of 1 mm, 100 um and 10 um (left to right). The fourth structure is a four-point probe structure. All features are ITO. ILD is removed everywhere.

5.13 Light Emission Test Structures

Two PLED test coupons were incorporated. The design is the same as in TV-1, i.e., insensitive to mask misalignment so the active area is always 1 cm^2. We provide ITO output pads, so that the environmentally sensitive cathode made of calcium aluminum sandwich can be encapsulated by a glass lid. The purpose of this structure is to separate processing problems of the NB backplane itself form difficulties of producing functional PLED structure on top of polymer layers used for the NB backplane fabrication.

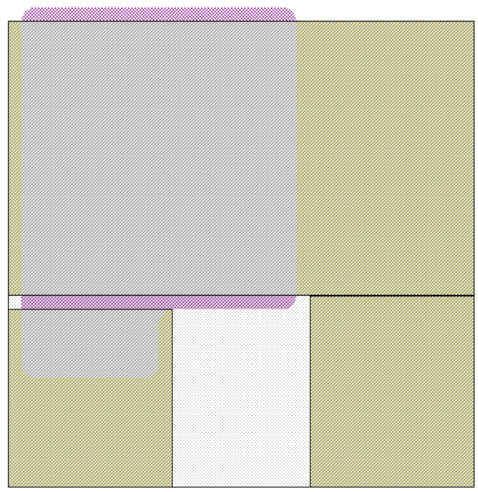


Figure 36. PLED test coupon. The left leg is the cathode electrode, the right leg is the ITO anode electrode. DISPLAYVIA2 is removed everywhere. There is a gap of 500 um between the cathode ITO contact and the ITO anode. The active device area is 10 mm x 10 mm.

5.14 Other Revisions

<u>Revision B</u>: Corrects slant of segments in 5 digit, 8 segment displays. As the display is viewed through the substrate, the figures need to lean the opposite way.

<u>Revision C</u>: Introduces Large Via layer for dual planarization layer approach and SiO_2 undercoat layer as a chemical barrier.

<u>Revision D</u>: Replaces ITO anode with molybdenum grid electrode plus PEDOT conducting polymer in between grid.

6. INTERFACE Electronics for TV-2

6.1 Design Specs and Rationale

TV-2 Electronics contains the following features:

- Interface with PLED displays on TV-2 backplane, consisting of a 5-digit 8-segment display & a 16x24 matrix display. (6 pins & 7 pins, respectively, on a 1mm pitch. Signals are in different locations for the 2 devices due to single layer metal on backplane.)
- Interface with a packaged Jade NB IC, housed in a 44-pin PLCC package.
- Interface with a test structure, TS1, which contains a wafer level Jade NB IC test structure (AMI structure, 39 pin probe card)
- Contain a sub-circuit that can be isolated and used in a portable demonstration device.

Additional requirements to accommodate Jade NB IC features:

- Clock must be capable of 1MHz to 100MHz operation with minimal revisions to hardware and firmware. The small time step is required to test the specification limits of the Jade NB IC.
- VDD (power line) must be capable of adjustment between 3V to 6V & able to supply a peak current of 300mA. Nominal currents range from 40mA to 80mA.
- VCOM (counter electrode) must be capable of adjustment between 0V to –2V and capable of sinking the current supplied to VDD. (Peak 300mA, 40-80mA nominal)
- Logic high for Clock & Data must track VDD in magnitude from 3V to 6V.
- VDD, GND, and Orient must be in-circuit configurable to simulate various rotations of the NB IC.
- Signals from Jade NB IC testing (Packaged or Wafer) should route to a header for probing and signal analysis.
- Outputs from Jade NB IC testing (Packaged or Wafer), in addition to the header for probing, should connect to a highly uniform 0.1% 10K resistor to measure output uniformity.

Based upon these requirements, a Xilinx field programmable gate array (FPGA) (XC2S100) & SPROM, serial programmable read-only memory (18V01), were chosen as the heart of the logic. The rationale is that the FPGA is capable of running with extremely fast clocks (up to 120MHz), whereas most other programmable logic devices execute instructions no faster than ~10MHz. The core logic of the Xilinx parts requires 3.3V and 2.5V to operate. Therefore, power supplies for 2.5V, 3.3V, VDD= 3-6V, and VCOM= 0-(-2)V are required. Since a sub circuit was targeted as a portable device, highly efficient (~75%) switching power supplies were designed. The alternative use of linear power supplies would achieve no better than 50% efficiency.

Instructions for the logic section were achieved using the Verilog programming language. Transfer of this information to the PROM and FPGA was accomplished through a 6-wire

interface, known as JTAG programming. Preliminary data patterns include: All on, All off, and a walking pattern throughout the 2 displays.

6.2 Schematics and PCB Layout

Schematics and PCB Layout are shown in Appendix G.

6.3 Obstacles to Completion and Recovery Plan

Unfortunately, Rev. A of the "Universal Tester Board" failed to operate. Failure analysis revealed several flaws.

- The VCOM circuit did not operate as it simulated. Apparently, there is a protection diode in one of the commercial ICs that prevents VCOM from going below –0.6V.

- The Xilinx FPGA had several pins mis-wired according to a working evaluation board that was obtained about the same time the design was completed.

Even after correcting these issues, the FPGA is not recognized by the JTAG programmer although the SPROM is.

Debug could continue and yield results, but may involve a board revision. A short-term solution was developed instead involving the evaluation board, shown in Figure 37. This

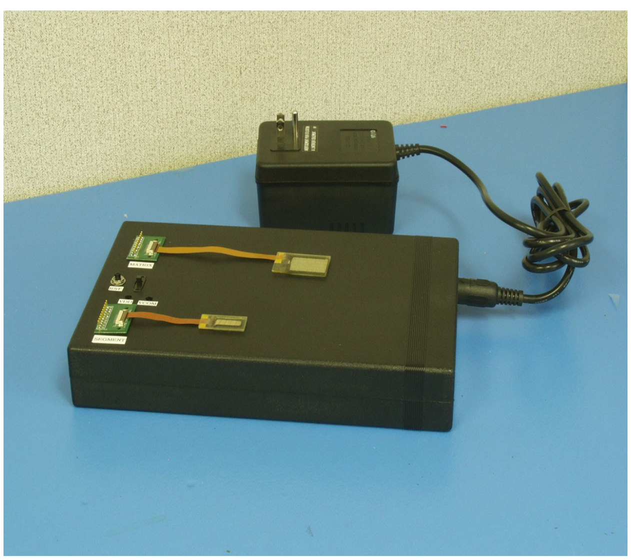


Figure 37. Completed Evaluation board shown with

unit already contains the myriad of complex logic for signaling and waveform generation. The addition of circuitry for VDD and VCOM will produce a functional test device so work on this display can continue. Furthermore, it will allow the refinements of firmware that may be required when driving a device. It is conceivable that a negative voltage on VCOM is unnecessary, thus eliminating circuitry and shrinking the portable device.

6.4 Recovery Plan Implementation Report

Circuitry for VCOM was implemented successfully using a bench top supply, but failed when driven by a single sided wall adapter. The shortcoming lies in the circuitry to generate a negative supply from a positive one. This problem was circumvented for this device by using a triple output power supply, providing a reliable –5V source. With this modification, the circuitry was implemented and two functional units have been built.

6.5 Future Work

If desired, improvements could be made in the electronics for the portable device (TV-2)

- Isolate the data stream from signal generation and develop a GUI interface for programming arbitrary pictures.
- Check portability of code to a more cost effective processor for portable devices (such as the PIC microprocessor), since no TV-2 device will require clock speeds greater than 5MHz.

7. PROCESS INTEGRATION

7.1 Introduction

The development of polymer light-emitting diode (PLED) direct driven display by embedded NB ICs requires the harmonization of two processes:

- The process for embedding the NB ICs into a flexible back plane with
- The standard PLED fabrication process.

The process proposed initially for formation of a backplane with embedded NB ICs is described in great detail in Appendix E. For the reader's convenience, a brief description is provided here. The process consists of following steps:

- *Molding* to produce the receptor sites in the embossing layer
- Fluidic Self Assembly (FSA) to seat the NB ICs into the receptor sites
- *Hot-press planarization* to remove the tilt of NB ICs
- *Spin planarization* to planarize the final surface of the backplane.
- ITO deposition and patterning
- Via opening (to connect display electrode to the contact pads of NB ICs)
- Metal deposition and patterning (to form the connecting wires)
- The standard PLED fabrication process.

A schematic cross-section of such a device is shown in Figure 38.

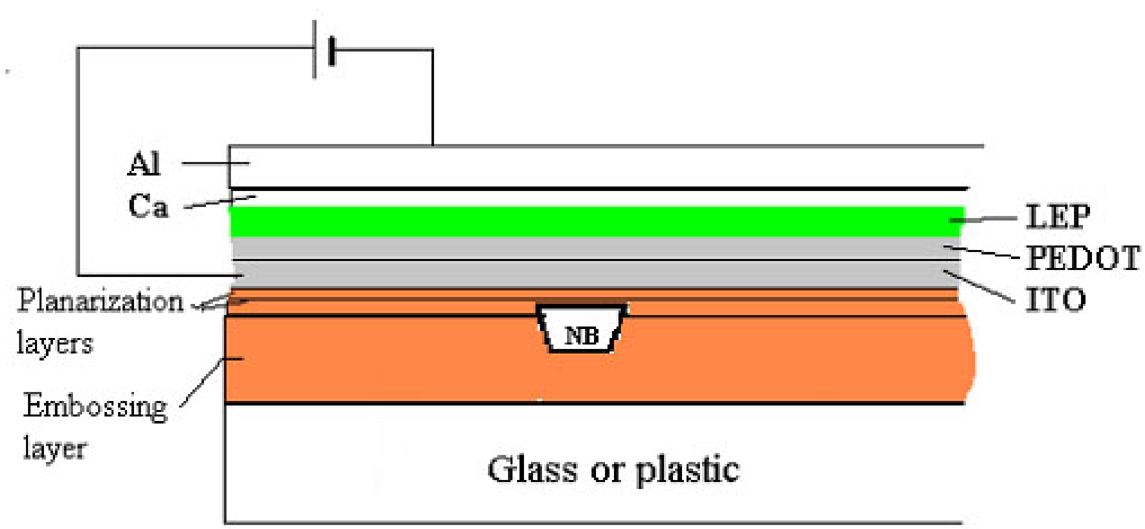


Figure 38. A schematic representation of PLED device built on flexible substrate with NB IC embedded in the backplane. Encapsulation not shown.

For PLED applications, the surface roughness of the backplane, the adhesion between the plastic and the ITO electrode, and the chemical and thermal stabilities of the back plane

materials are all major concerns. The actual quality of the finishing surface of the back-plane depends on the process conditions as well as the intrinsic physical and chemical properties of the material(s) used. In the Alien Standard Manufacturing Process at the time of this project, Norland 83H adhesive (NOA83H) is used for the embossing layer, hot-press planarization layer, and the spin planarization layer. For a flexible PLED display using this approach, it would be required to deposit ITO and build PLED devices on the surface of a NOA83H coating. In order to evaluate the suitability of NOA83H as the backplane material for this application, we first built test PLED devices on glass substrates coated with a single layer of NOA83H (~10μm thick). We invested considerable effort in this area, as we desired to make our PLED fabrication processes as compatible as possible with the considerable expertise existing within Alien around the Norland-compatible process and design.

7.2 PLED on Norland Adhesive

The fabrication of such devices includes spin-coating of NOA83H on a glass substrate, curing of the NOA83H coating, sputter deposition and patterning of ITO, and standard PLED device fabrication process. The first problem encountered in this process was the poor adhesion between the ITO and the NOA83H surface. It was found that the ITO film does not survive our standard ultrasonic bath cleaning procedure. In fact, even the spray-water rinse cleaning procedures could sometimes remove the ITO film from the NOA83H surface. In order to make a complete device from such substrates, we had to abandon the standard ITO cleaning process. As a result, the finished PLED devices suffered large leakage current (rectification ratio Ifwd/Irev<10), high working voltage (~40V @ 10mA/cm2), low efficiency, and non-uniform emission with large amount of black spots across the active area. An example of such poor performance characteristics is shown in Figure 39, and the physical appearance in Figure 40.

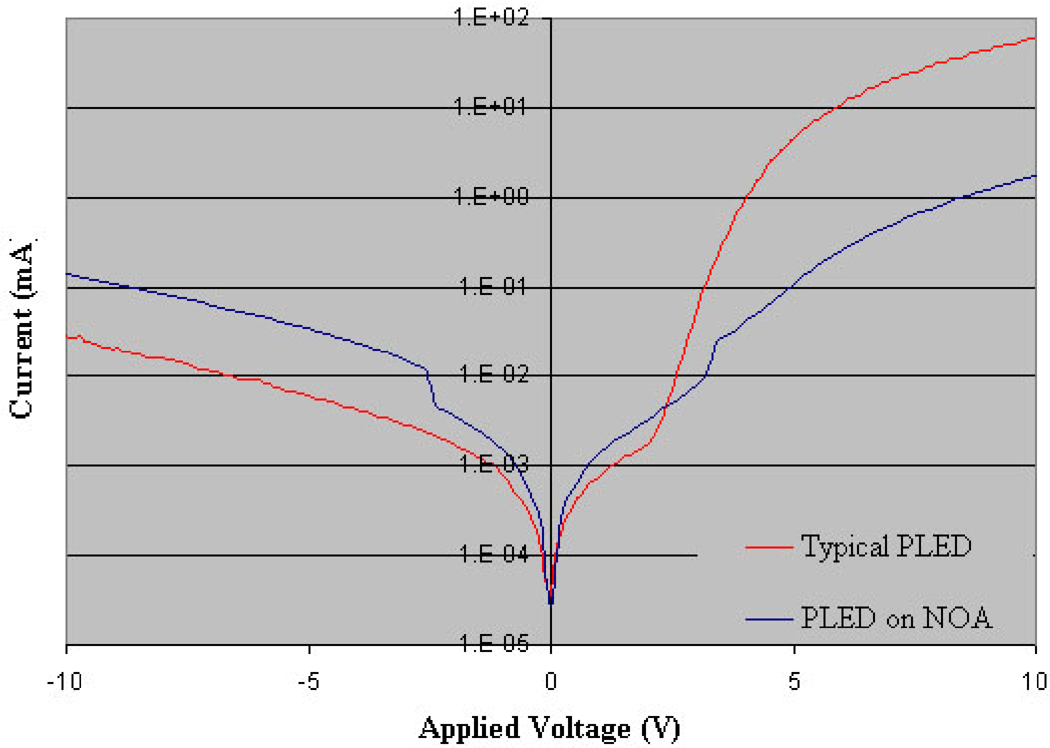


Figure 39. I-V curves of a typical PLED device built on a glass substrate and a device built on an NOA83H coated glass substrate

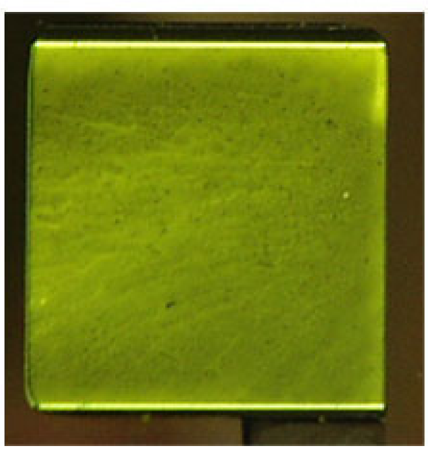


Figure 40. A comparison of a PLED device built on NOA83H coated glass substrate (left) and a regular device built on soda lime glass (right).

The poor appearance and performance of the above device is caused by following:

i) Rough ITO surface
The high leakage current observed in the above device indicates the existence of large amount of pinholes, which is usually the result of a rough ITO surface. It is generally known that the average roughness (Ra) of the ITO used in PLED applications should be 5 nm or less. However, the Ra value of the ITO films deposited on NOA83H surface is nearly 200 nm, i.e., 40 times over the acceptable value of 5 nm.

The conductivity of these ITO films is also poor, as shown in Table 8.1. The resistance of an ITO film deposited on PET (Mylar) is only 10-20% higher than that deposited on a glass substrate. The ITO film deposited NOA83H, however, has more than one order of magnitude higher resistance then the control sample (ITO deposited on glass). Since the thickness (80nm) of the ITO film is smaller than the Ra value (~200nm) of the ITO surface, it is obvious that the discontinuity of the ITO film is the major contributor to the high sheet resistance. The surface roughness was typically established by surface profiler based on optical interference (Figure 41.).

Table 2. Conductivity of ITO film deposited on different materials.

	From Vendor	Deposited in House (thickness of film = 80nm)
On Glass	~ 10 Ω/sq. (Applied Films, thickness =130nm)	60-80Ω/sq.
On PET film	50-80 Ω/sq.	80-90 Ω/sq.
On NOA83H		~ 1 k Ω/sq.

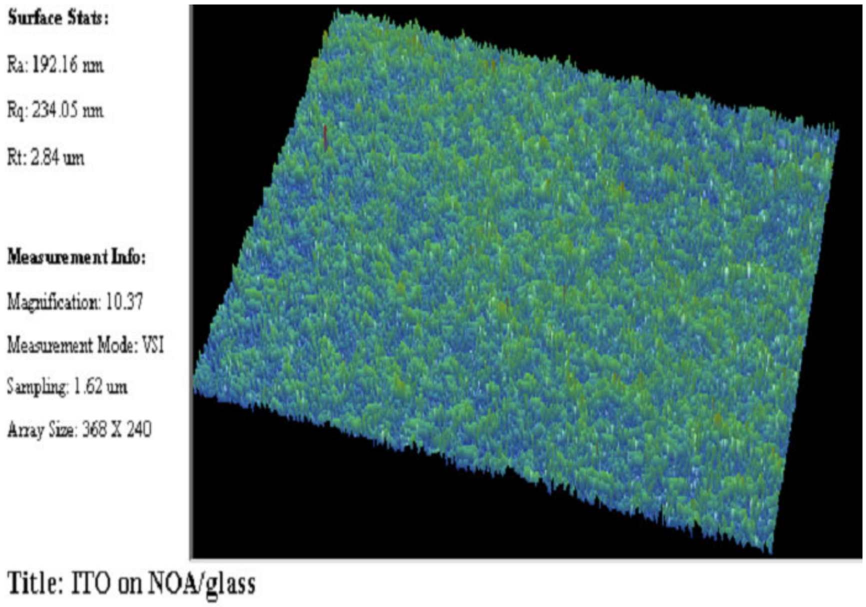


Figure 41. Surface roughness of ITO film (~1200Å) deposited on NOA83H determined with WYKO interferometer.

ii) *Dirty ITO surface*

Although it is expected that the poor conductivity of the ITO anode could increase the device operating voltage to a certain extent, at low current density this increase should be insignificant. Thus, the unusually high operating voltage (~40V!) of the device could not be simply attributed to the increase of the ITO sheet resistance alone. A specially designed PLED pattern (Figure 42) reveals some insight of this phenomenon. Shown on the left of Figure 42 is a PLED device built on NOA83H coated glass substrate. The unusual appearance of this device can be easily seen when compared to the normal device shown on the right: the area without ITO (but near the ITO electrode) emits much more strongly then most ITO area! This could be a result of ITO surface contamination by an insulating material, and/or there was no PEDOT coated on the ITO surface. Since PEDOT solution usually wets the clean ITO surface very well, the latter case also indicates that the ITO surface is contaminated by a hydrophobic contaminant. Although it is still not clear at this time what the contaminant is, some of the possible contamination sources are i) residual photoresist, ii) NOA83H which was partially dissolved in the Safestrip solution during the photoresist stripping process, and/or iii) the decomposition products of NOA83H during the ITO etching process (i.e. the decomposition products were dissolved and re-deposited on the ITO surface by the Safestrip).

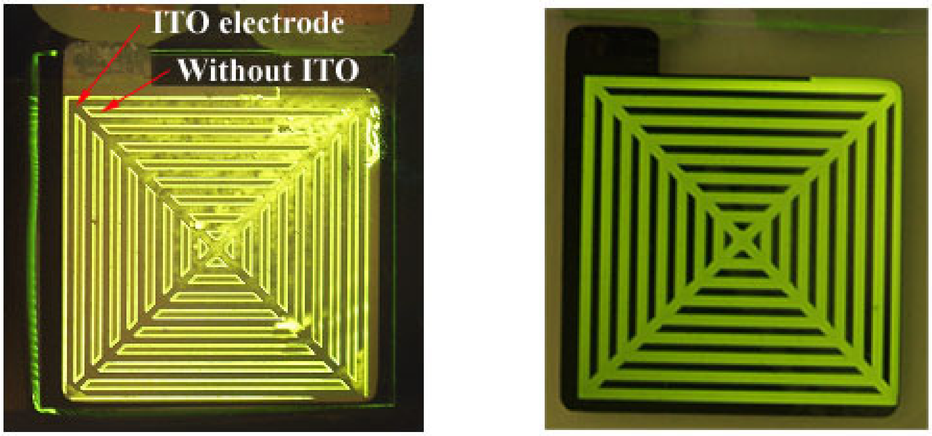


Figure 42. Comparison of a PLED device built on NOA83H coated glass substrate (left) and a regular device built on soda lime glass (right).

In summary, the major problems of NOA83H being used in PLED applications are i) rough surface, ii) poor adhesion to ITO, and iii) poor chemical resistance. In addition, it is also know from the previous experience that NOA83H has other problems such as out-gassing and large shrinkage, which are also harmful to PLED devices. As such, an alternative approach was warranted.

Some possible solutions for these problems are:

- use a different material for planarization layer to planarize the surface of the underlying NOA83H, or,
- Completely replace the NOA83H in the whole NB back plane structure or,
- Use the “tri-layer” approach to protect the ITO surface from being contaminated during the ITO patterning process (described later in Chapter 8.5).

7.3 Search for Better Planarization Material

The requirements for the FSA-compatible planarization material are:

- Transparency
- Smooth surface (Ra<5nm)
- Good adhesion to glass, plastics, ITO, and Al
- Proper viscosity for spin coating (<2000 cps)
- UV or heat curable
- Thermally and chemically stable after curing
- Patternable (wet etch, dry etch, etc.)
- Good chemical resistance to acids and solvents.

Two approaches were considered at this juncture. One approach was to develop a custom polymer in cooperation with a chemical company; the other approach was to screen

available commercial polymers and choose the best performer. Given the wide variety of suitable products easily available in the market, we have chosen the latter approach for its speed and independence of a potential partner.

Our search for such replacement material was conducted in three stages:

- material screening,
- detailed physical/chemical properties study,
- optimization of the backplane structure.

7.3.1 Material Screening

In the Stage 1 (material screening), the potential candidates were spun onto glass substrates and fully cured. The surface roughness of the coatings was then determined. If the surface roughness of the coating was satisfactory, a quick test on the chemical resistance to organic solvents and acids (by visual inspection) was performed.

Table 3. Surface roughness of different materials

Material	Ra	Rq	Rt	Color	Coating Technique	7.3.1.1.1.1 Chemical Resistance	
						Safestrip	ITO etchant
Comm. PET	9 nm	17 nm	1820 nm				
Comm. ITO/glass	5 nm						
NOA83H on glass	90 nm	115 nm	800 nm	Colorless	spin-coating		
ITO on NOA83H/glass	217 nm	234 nm	2840 nm	Colorless	spin-coating		
NOA61 on glass	35 nm	42 nm	250 nm	Colorless	spin-coating		
NEA121 on glass	6 nm	8 nm	180 nm	Colorless	spin-coating		
SP-22 resist on glass	107nm	133 nm	680 nm	green	Screen printing	yes	yes
SP-22 resist on glass	7 nm	10 nm	136 nm	green	spin-coating	Al lifted off surface after one week. Chemical reaction?	
Sumitomo Bakelite (-P.R.), CFP-1123	100 nm	153 nm	5630 nm	white	lamination		
Carapace EMP110	250 nm	415 nm	4790 nm	white	spin-coating		
Tiayo 9000 6RW on glass	235 nm	278 nm	5430 nm	dark green	Screen printing		
SC Neg Resist on glass	7 nm	10 nm	185 nm	yellow	spin-coating	no	no
OG112 on glass	6 nm	9 nm	163 nm	colorless	spin-coating	yes	yes
RC20-169	>> 100 nm			white	spin-coating		
Epo-Tech OG142	26 nm	31 nm	176 nm				
Epo-Tech OG169	6 nm	8 nm	150 nm	colorless	spin-coating	yes	yes
Epo-Tech OG114-4	5 nm	n/a	n/a	colorless	spin-coating	yes	yes
Epo-Tech OG133	70 nm	80 nm	670 nm	colorless	spin-coating	yes	no
Epo-Tech OG604-5	Viscosity too high to spin; not soluble in safestrip						
Epo-Tech OG198-50	Cured in 500 seconds (OAI); many particles (polymerized unevenly?) Try to filter it?						
Master Bond UV15	35nm	45 nm	447 nm	colorless	spin-coating	yes	yes
Master Bond UV15-7	9 nm	11 nm	190 nm	colorless	spin-coating	yes	no
Master Bond UV15-7sp4	22 nm	27 nm	250 nm	colorless	spin-coating	yes	no
Master Bond UV10 LV	>>100 nm			colorless	spin-coating		
Master Bond UV10 LV diluted with Acetone	7 nm	9 nm	141 nm	colorless	spin-coating	yes	no
Master Bond UV10 LV diluted/safestrip	7 nm	9 nm	144 nm	colorless	spin-coating	yes	no
Master Bond UV10 MED	>> 100 nm			colorless	spin-coating		
Master Bond UV10 MED diluted/acetone	8 nm	11 nm	222 nm	colorless	spin-coating	yes	no
Master Bond UV10 MED diluted/safestrip	8 nm	10 nm	173 nm	colorless	spin-coating	yes	no
Master Bond UV10	>> 100 nm			colorless	spin-coating		
Master Bond UV10 diluted/acetone	7 nm	9 nm	170 nm	colorless	spin-coating	yes	no
Master Bond UV10 diluted/safestrip	9 nm	11 nm	229 nm	colorless	spin-coating	yes	no
MicroChem SU8	5 nm	N/a	N/a	colorless	spin-coating	yes	yes

Ra: the average roughness; Rq: the root mean square roughness; Rt: the peak-to-valley difference.

Over twenty materials from several different vendors were examined in Stage 1. Results are summarized in Table 3. The materials that passed the Stage 1 tests are OG112, OG169,OG114-4 UV epoxies from Epoxy Technology, and the SU8 negative photoresist from MicroChem Corp. The SP-22 negative photoresist also passed the screening. It was

found later, however, that it has a poor adhesion to Al and thus was not considered for further work. Candidates that passed the above preliminary tests were then tested in more detail in the Stage 2 study.

7.3.2 Detailed Material Evaluation

In the Stage 2, the physical and chemical properties of the materials were studied in more detail. This included the adhesion of the materials to the ITO film and to the substrate, the thermal and chemical stabilities of the materials, the quality of PLED devices constructed on these materials, the feasibility of using the materials as the embossing layer, hot-press planarization layer, spin-planarization layer, and other related issues. Some physical properties of ITO thin film (1250Å) deposited on different materials are summarized in Table 4. More detailed discussions on these results are found in the following sections.

Table 4. Physical Properties of ITO films Deposited on Different Materials

Substrate #	**R (Ω/□)**	**T%**	**Layer Structure**	**Ra (nm)**
Control sample	39	94	Glass/ITO	4, 4, 4
Zircon 1006-1	43	92	Glass/NOA/114/114/ ITO	5, 7, 5
Zircon 1006-2	42	92	Glass/NOA/112/112/ITO	9, 5, 100
Zircon 1006-3	41	92	Glass/NOA/114/114/ITO	6, 10, 10
Zircon 1006-4	43	92	Glass/NOA/112/112/ITO	4, 9, 20
Zircon 1006-5	41	91	Glass/NOA/NOA/112/ITO	5, 33, 100
Zircon 1006-6	42	91	Glass/NOA/NOA/114/ITO	5, 4, 3
Zircon 1006-9	42	89	ITO/169/169/169/glass	n/a, 13, 20*

* The three R_a values shown in the last column are (from left to right): the Ra of epoxy surface before ITO deposition, of the ITO surface after ITO deposition, and of the ITO surface after ITO film is patterned , respectively. Abbreviations used in this table: 114 = OG114-4 UV epoxy; 112 = OG112 UV epoxy; 169 = OG169 UV epoxy; NOA = NOA83H Norland adhesive. ITO was deposited at 800W DC. Thickness of ITO films is approximately 125nm. Zircon refers to a different NanoBlock IC structure that was used for these tests.

7.3.2.1 SP-22 Resist

Shown in Figure 42 is a PLED device built on a glass substrate coated with NOA83H and subsequently planarized with SP-22 photoresist (spin planarization). After the SP-22 resist was fully cured, ITO was deposited and patterned using the standard procedure. Due to adhesion problems, the substrate was used directly after the ITO patterning process without receiving the standard ultra-sonic cleaning procedure. Although the device performance is still unsatisfactory, improvements are easily seen when compared to the PLED device built directly on NOA83H (Figure 43). Firstly, the operating voltage of the device is significantly lower; secondly, the device emits light as expected (i.e. from areas delineated by the ITO anode), and thirdly, the emission is more uniform. This indicates that the SP-22 has better chemical resistance to the ITO etchant and/or to the Safestrip. Due to the fact that the deposited Al tends to lift off the SP-22 surface upon aging (in approximately two weeks), no further study was performed on this material.

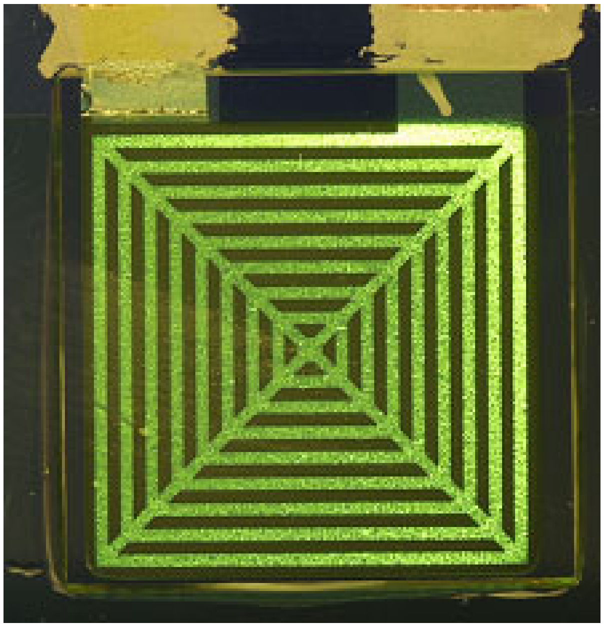


Figure 43. PLED device built on NOA83H planarized with SP-22 resist. The NOA83H was spun on glass substrate

7.3.2.2 OG112 UV Epoxy

a. *The Embossing Layer*

The casting procedure for OG112 epoxy is compatible with that of NOA83H, except that OG112 requires longer curing time. Receptor site quality was judged either similar to those formed in NOA83H, or better. However, the embossing layer delaminated during the pre-FSA plasma etching process. Although it is expected that adhesion could be improved by plasma treatment of the glass substrate prior to casting, the epoxy OG112 was not further considered for embossing layer because of other available choices.

b. The Hot-press Planarization

When used for hot-press planarization on other test substrates with other types of embedded NB ICs (Alien's Zircon liquid crystal driver NanoBlock IC) in NOA83H, small surface ridges above and along the NB IC periphery (boundary peaks) were found on the OG112 surface. The typical height of these boundary peaks is < 2m (Figure 44).

It should be noted that the heat anneal (90 °C in air for 20 minutes) following the hot-press planarization raises the boundary peak height by 2-3m. Since large boundary peaks will cause serious streaking in the spin planarization layer (which follows the press planarization), we decided to perform the annealing process after the spin planarization (and not before as it's done in the Standard Manufacturing Process).

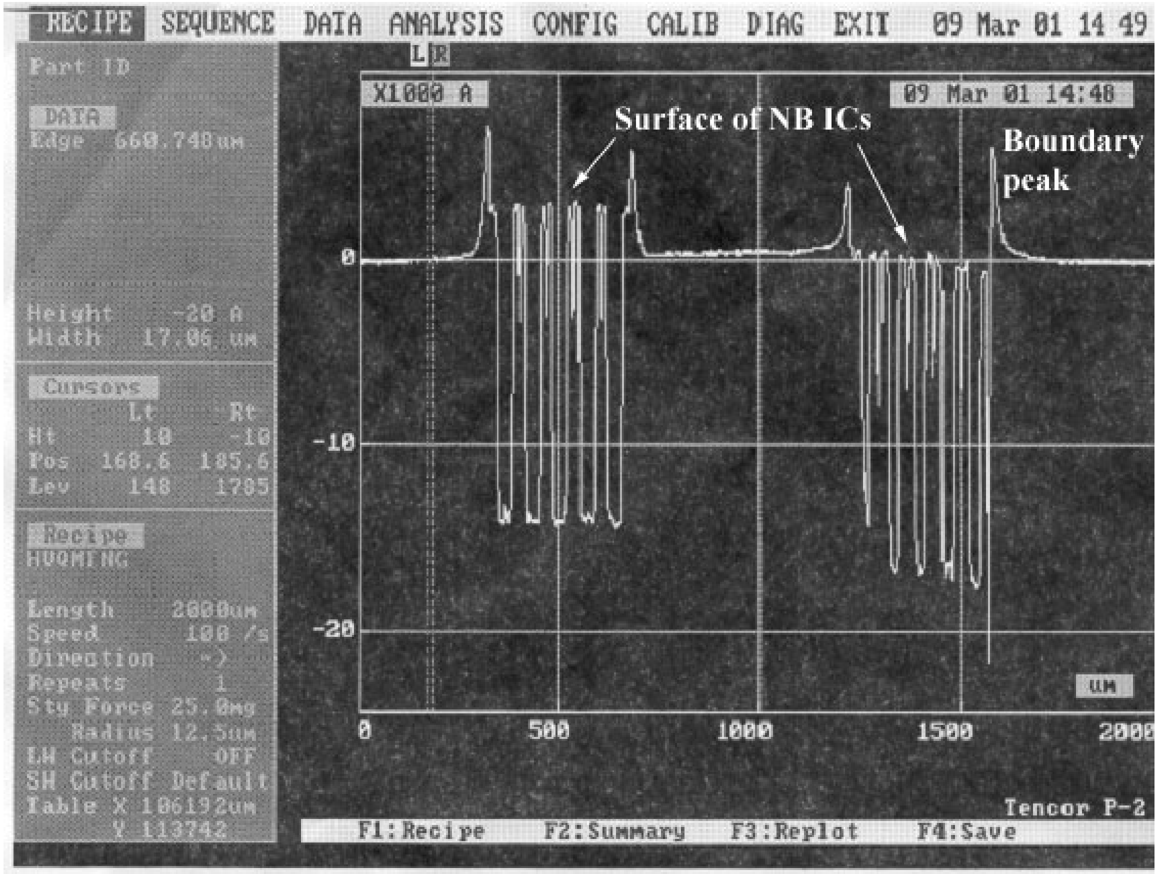


Figure 44. Surface profile of a Zircon substrate hot-press planarized with OG112 UV epoxy. (Tencor profilometer)

c. Spin planarization

OG112 can satisfactorily planarize surfaces with bumps of several um high, regardless whether the substrate was hot-press planarized with NOA83H or OG112 (Figure 45). At areas heavily populated with NB ICs, the resulting surface had valley-to-peak height of 0.8 ~1.6□m with adjacent valley-to-valley distance of 1000□m (the distance between the adjacent NB ICs such as within certain test structures on TV-2 substrate).

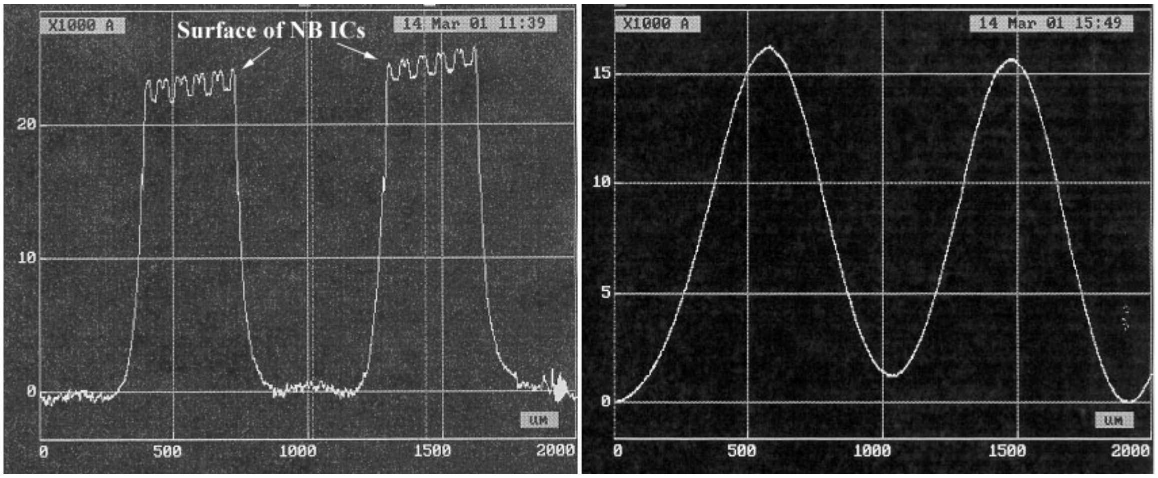


Figure 45. Shown on the left is the surface profile of a test substrate. The trace en-com-passes two NB ICs after hot-press planarization with NOA83H and annealed at 90ºC for 20 minutes. Shown on the right is the same area after spin planarization with OG112 UV epoxy

d. *Deposition of ITO on OG112*
The surface wrinkles previously seen on the NOA83H layer were also observed on an ITO layer deposited on top of the OG112. As a result, the surface roughness has increased after ITO deposition, especially when there is only a single layer of OG112 on top of the NOA83H layer (see Table 4 and Figure 46). These surface wrinkles became even more pronounced and the surface roughness increased even more (Ra ≈ 100nm; Rt ≈ 300nm) after the ITO was patterned (see results summarized in Table 4). In another separate experiment, ITO was deposited on a glass substrate coated only with OG112. Although similar surface wrinkle pattern was also observed, the resulting ITO film has much lower Ra value. The fact that substrate #1006-4 and #1006-2 have different Ra values (Table 4) is most likely due to the thickness difference in the OG112 layers.

It was found that reducing the power level during ITO deposition (sputtering) can significantly reduce this surface-wrinkle phenomenon. For example, when ITO was deposited at 400W DC (1/2 of the standard power), no significant wrinkles were seen on the resulting ITO film deposited on OG112. For the sake of consistency, the ½ power (400W DC) was used as the default for ITO deposition for all experiments discussed in this report, unless otherwise noted. We hypothesize that the wrinkles are formed due to excessive stress built in the ITO layer during faster deposition.

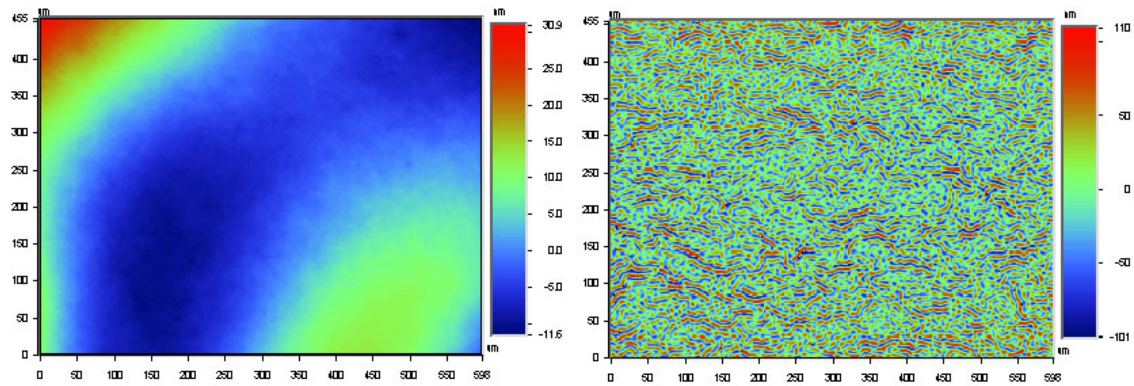


Figure 46. Left: The surface of OG112 layer spun on NOA83H before ITO deposition. Right: After ITO deposition, i.e., the surface of deposited ITO film.

e. *Performance of PLED built on OG112*

PLED devices constructed on OG112 suffered with two major problems: surface wrinkles and the contamination of the ITO anode. These features caused large leakage currents, high operating voltage, and highly non-uniform emission (Figure 47). Although the ITO wrinkle problem has been corrected by reducing the magnetron power during ITO sputtering, we did not find a reliable way to clean the ITO surface without damaging the ITO film. The direct results of contamination present on the ITO surface are increased anode resistance and poor wetting of PEDOT solution of the anode surface. The picture shown on the left of Figure 48 clearly shows that PEDOT was not coated on the whole ITO electrode, indicating that the PEDOT solution did not wet the anode. Extended UV-ozone treatment prior to spin-coat of the PEDOT solution achieved some improvement, but this approach was not sufficient to remove heavy contaminations. For example, in the device shown on the right of Figure 48 the ITO received 45 minutes of UV-ozone treatment (standard for ITO on glass is 15-20minutes). It can be seen that most of the ITO electrode is still covered by the contaminant.

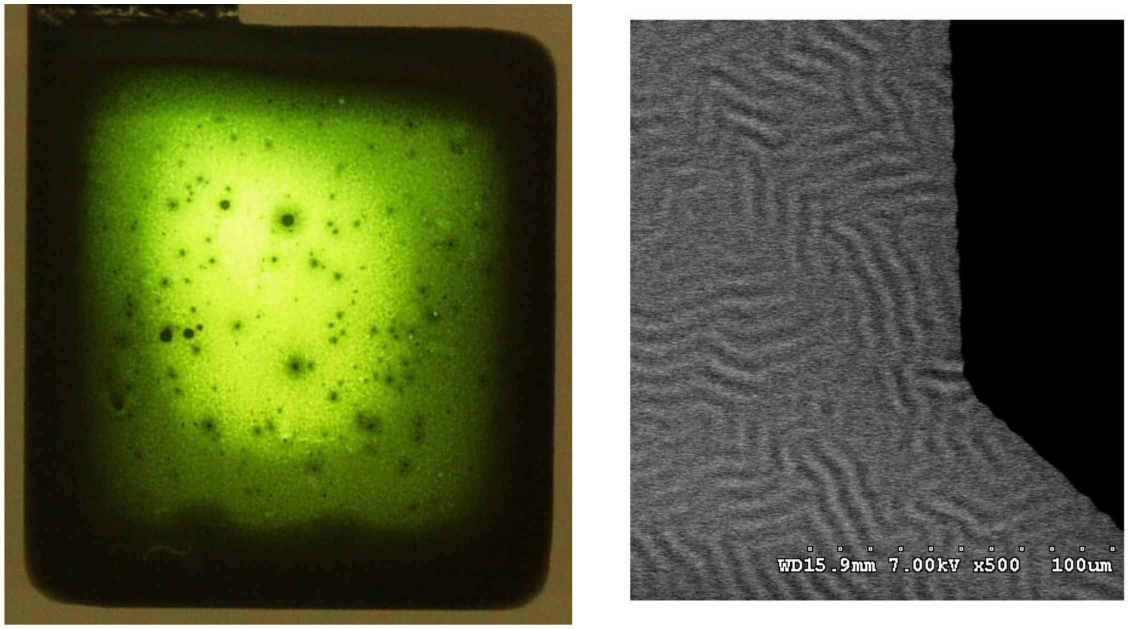


Figure 47. Left: PLED device built on a test substrate planarized with OG112 (glass with NOA83H as the embossing layer). Right: SEM image of the wrinkled surface of an ITO film (gray) deposited on OG 112 surface.

It was found that the ITO film deposited on OG112 did not survive the ultrasonic cleaning procedure, despite the observation that OG112 has shown better adhesion to ITO film than the NOA83H. It was thus concluded that OG112 is not suitable for the top planarization layer (the layer which is directly in contact with ITO).

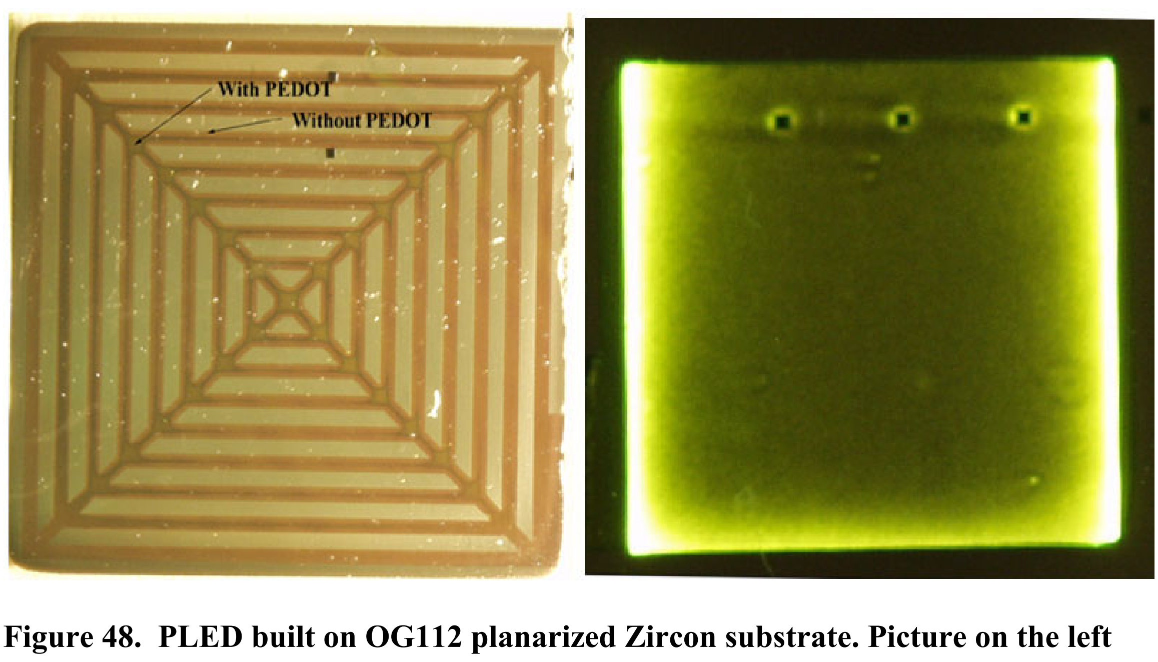


Figure 48. PLED built on OG112 planarized Zircon substrate. Picture on the left showed that PEDOT solution did not wet the ITO electrode; picture on the right showed a finished PLED device.

7.3.2.3 OG169 UV Epoxy

a. *The Embossing Layer*

Similar to OG112, OG169 also requires longer UV curing time than NOA83H. The quality of receptor sites was similar to those formed in NOA83H, or of better. Its adhesion to glass surface is better than OG112 but still unsatisfactory. From total 15 substrates molded with OG169, 30% of them delaminated before or during FSA process. Thus OG169 was not considered to be the best choice for the embossing layer when used on a glass substrate.

b. *Hot-press planarization*

When compared to OG112, the boundary peaks for OG169 are significantly smaller. Depending on the material used for the embossing layer, the boundary-peak height varies from 0.0 to 0.8□m. The typical boundary-peak height observable on the OG169 surface (after hot-press planarization) is <0.5□m. Similar to the other materials, the heat anneal (90 °C for 20 minutes in air) also raises the boundary-peak height by 1-2□m. Among the three UV epoxies tested, OG169 is the best for hot-press planarization if the boundary-peak height is a major concern (Figure 49, picture on the left).

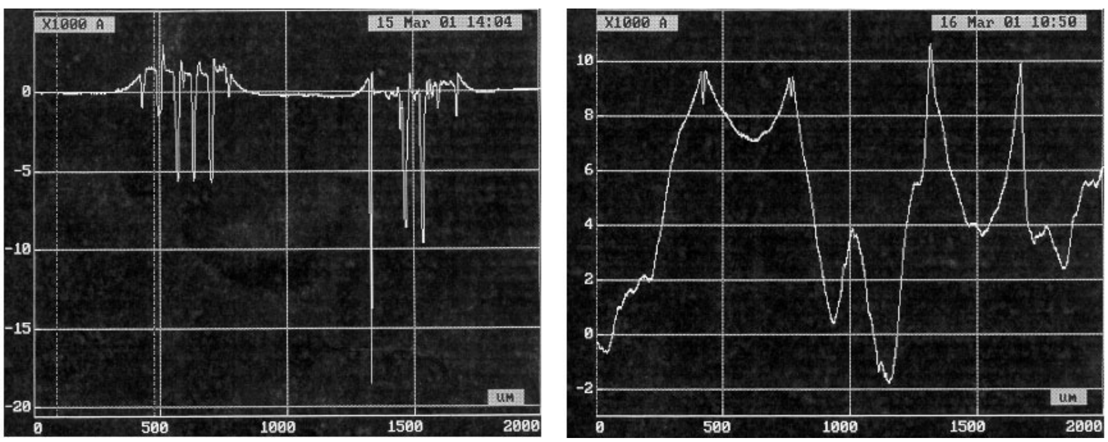


Figure 49. Left: Test substrate after hot-press planarization with OG 169. Right: same substrate with spun-on OG169, then transferred into a N2 glovebox via antechamber using three pump/refill cycles, and finally cured inside the glovebox

c. *Spin planarization*

When OG169 was spun onto the above substrate and cured under nitrogen in a glovebox, the resulting surface showed unpredictable irregular bumpy features (Figure 49, picture on the right), with maximum peak-to-valley height of 4µm. This phenomenon was not seen in OG112 but was also observed in OG114-4 (see below). We suspected that the roughening of the surface occurred inside the antechamber of the glovebox during the pump/refill purification cycles. Since OG169 has much lower viscosity than OG112 and contains a significant amount of components with low boiling point, these components and/or the dissolved gases try to escape (under vacuum) in the form of bubbles, damaging the smooth surface of the coating. This assumption was later confirmed.

This phenomenon was eliminated when we applied the following modifications to the process: i) use longer pre-spin plasma etching time and ii) instead of using the antechamber's regular pump/refill purification cycles which expose the uncured epoxy to low vacuum, use continuously purged mini-antechamber with N2 for 10 minutes (later we cured the substrate in a special UV chamber continuously purged with N2). Due to its lower viscosity, OG169 is only good for planarizing surfaces of lower roughness (Rt of sub-micrometer scale).

d. *Deposition of ITO on OG169*

Although no significant surface wrinkles were observed on the ITO film sputtered at standard power level (800W DC) on OG169 before and/or after ITO patterning, for consistency reasons ITO layers used in all following experiments were deposited at half power (400W DC). The adhesion of ITO to OG169 is better than to OG112. After the post via-etch ultrasonic cleaning (1 minute), the patterned ITO is still present on the substrate. However, many defects ranging in size from microns to sub-microns were observed on the ITO (Figure 50). These defects were not seen before the ultrasonic cleaning. The sheet resistance also increased from 42 Ω/☐ (before cleaning) to ~1000 Ω/☐m (after cleaning). This is most likely due to the lifting of ITO film from some areas of the epoxy surface, an indication of unsatisfactory adhesion between ITO and OG169.

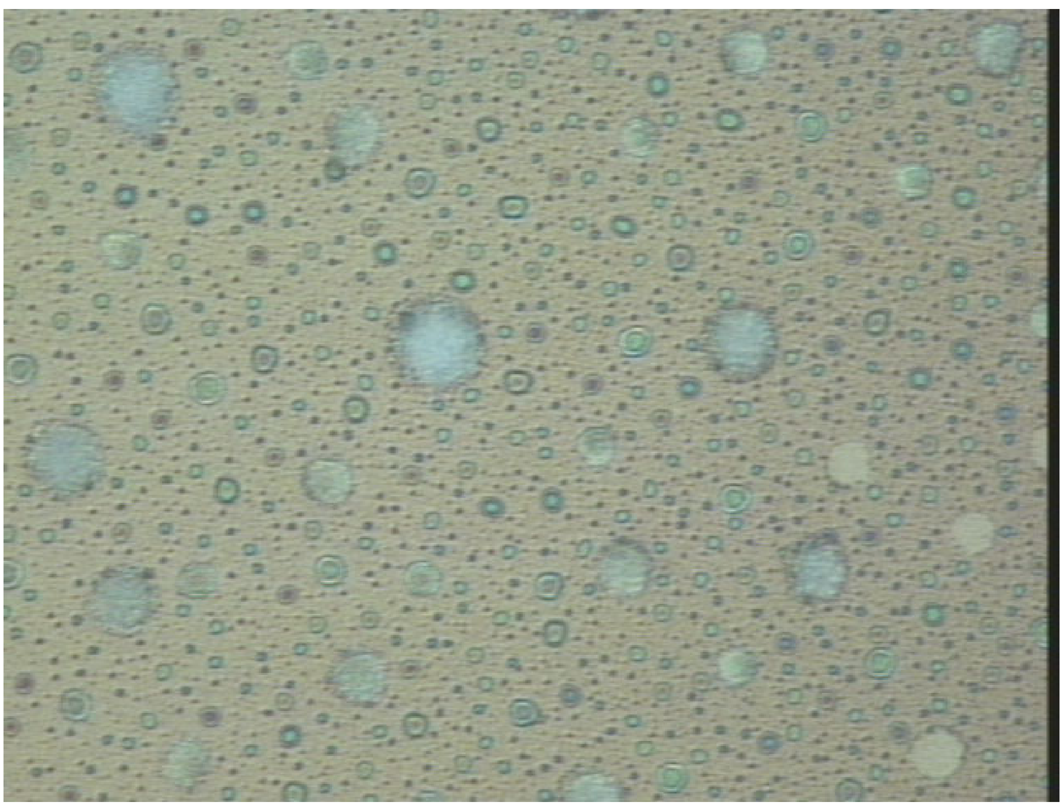


Figure 50. ITO on OG169 after ultrasonic cleaning for 1 minute (Optical microscope, 500x).

7.3.2.4 OG114-4 UV Epoxy

a. *The Embossing Layer*

The receptor sites formed in an OG114-4 layer have essentially the same size as the mold, indicating almost no swelling of the OG114-4 layer during cure. Therefore the rules previously used for designing the mold were designed to reflect the OG114-4 dimensional stability. The redesigned new mold for OG114-4 is only 2μm larger than the dimension of the NB IC to be used, which is the target value for the proper sized receptor site.. Among the three epoxies discussed above, OG114-4 has also the best adhesion to the glass substrate. All substrates molded with OG114-4 were successfully processed at the FSA machine without delamination.

b. *The Hot-press Planarization Layer*

The boundary-peak height is similar to that of OG112, which varies from 1 to 3μm on a substrate with NOA83H as the embossing layer and OG114-4 as the hot-press planarization layer. Heat anneal (90 °C for 20 minutes in air) raises the boundary-peak height by additional 1-4μm.

c. Spin planarization

Spin-coating of OG114-4 on a NOA83H surface (hot-press planarization layer) significantly reduces the bumps created by the embedded NB ICs. Shown in Figure 51 are the surface profiles of such a substrate before (left) and after (right) the spin planarization using OG114-4. It can be seen that the bump height was reduced from ~3μm to ~0.4μm after the spin planarization.

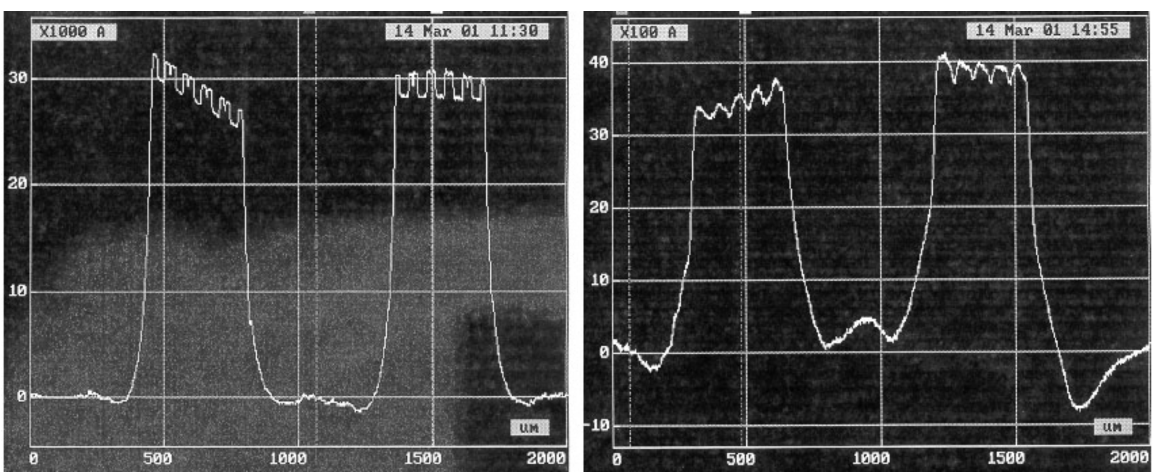


Figure 51. TV-2 substrate before (left) and after (right) spin planarization with OG114-4 UV epoxy (thickness »12mm). NOA83H was used for both the embossing layer and the hot-press planarization layer.

Interestingly, when we tried to spin OG114-4 over a surface of an OG114-4 film, unpredictable and irregular bumpy features were observed (Figure 52). The typical peak-to-valley height of the resulting surface was ~4μm, sometimes extending the range even further (10-15μm deep, ~100μm wide as shown in Figure 52, left picture). This phe-

nomenon is similar to what has been seen previously in OG169, but more severe. Fortunately, these problems can also be corrected by the process modifications previously used for OG169: i) use longer pre-spin plasma etching time and ii) instead of using the antechamber's regular pump/refill purification cycles which expose the uncured epoxy to low vacuum, use continuously purged mini-antechamber with N2 for 10 minutes; or cure the substrate in a special UV chamber continuously purged with N2 gas at the atmospheric pressure.

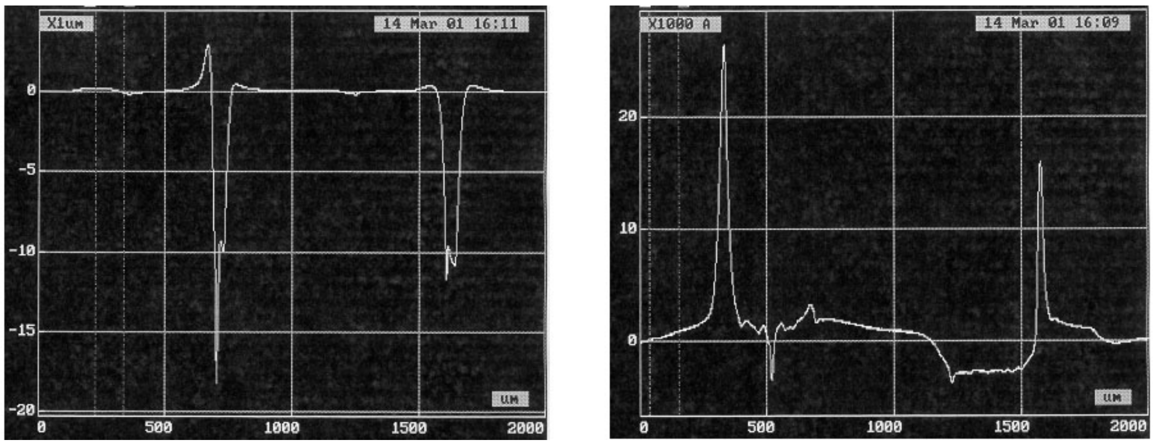


Figure 52. Examples of various surface features observed on OG114-4 spun on another layer of OG114-4 and cured in glove box. Left: 10 to 15 mm deep valleys. Right: 1.5 to 2.5 mm bumps.

d. *ITO deposition*

The surface smoothness did not change after ITO deposition, or after ITO patterning even when ITO was deposited at the standard power level (800W DC). After the post via-etch ultrasonic cleaning, defects similar to those previously seen in ITO deposited on OG169 are also observed. However, the size of these defects was smaller, at sub-micro level, which may suggest that the ITO-epoxy adhesion is somewhat better than OG169. As expected, the ITO sheet resistance also increased, but to a lesser extent - from 42 Ω/square to 140 Ω/square.

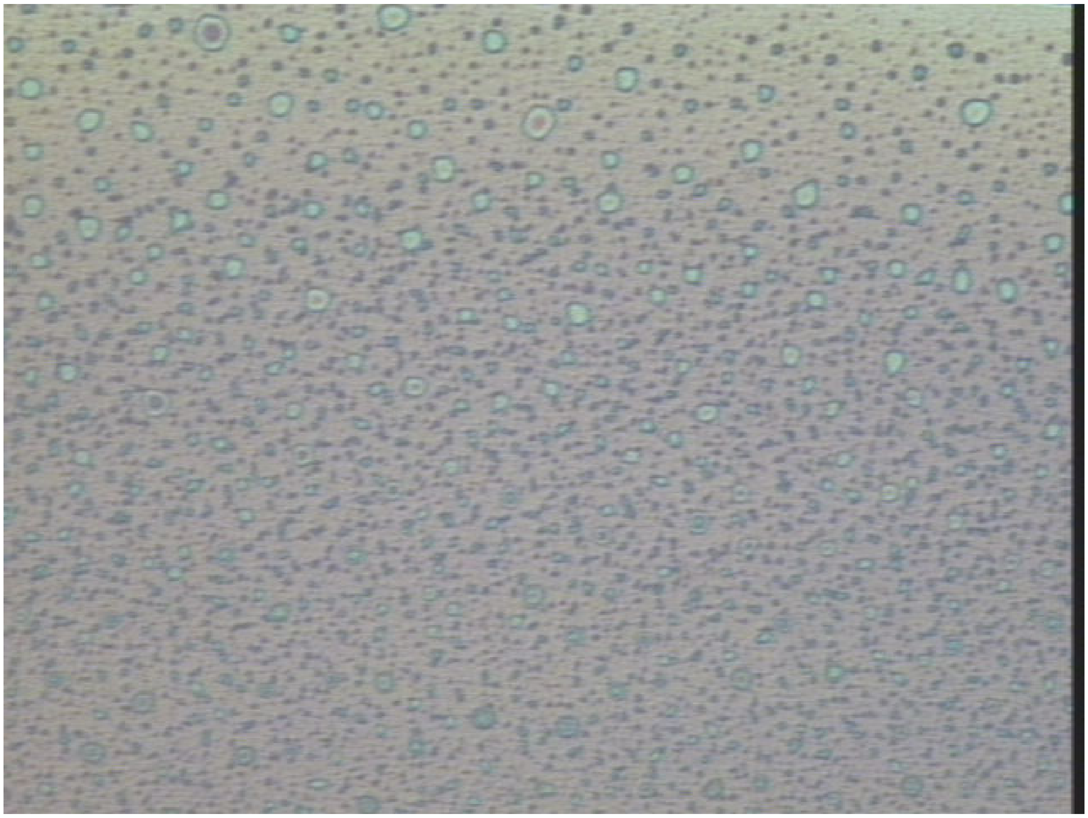


Figure 53. ITO on OG114-4 after the post via-etch ultra-sonic cleaning for 1 minute (Optical Microscope, 500x)

7.3.2.5 SU8 Photo-imageable Epoxy

a. Spin Planarization Layer

The SU8 is an epoxy-based negative photoresist containing an organic solvent. It is available in various viscosities, depending on the solvent contents (Table 5). We observed during our screening experiments that the surface of a spun-on SU8 film is generally very smooth (Ra=2nm). The surface smoothness is not affected by the ITO deposition even when using the standard power level (800W DC). It also exhibited very good adhesion to the deposited ITO film (no defects can be seen after up to 10 minute ultrasonic cleaning) and good chemical resistance to ITO etchant as well as to the Safestrip (Figure 54). All these characteristics made it an excellent material for the top planarization layer. Since it contains an organic solvent, it is currently impossible to use it for the embossing and hot-press planarization. In the various formulations listed in Table 5, SU8-10 has the proper viscosity for planarizing the TV-2 substrates, which usually have vias of several to 10 μm deep. On the other hand, SU8-5 can planarize smoother surfaces with Rt in the range of sub-micron or less without causing marked streaking. Due to its lower viscosity, it is not recommended for surfaces with Rt of microns or higher using the spin-coating technique. An additional benefit of SU8 is its photo-imageability, which allows to form the vias by photolithography (as opposed to the current dry etching approach).

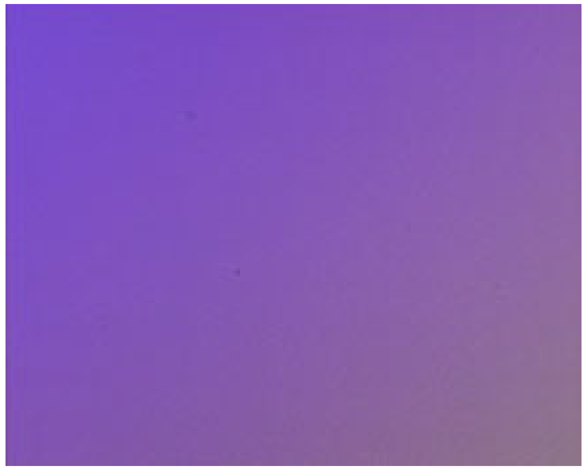


Figure 54. Featureless surface of ITO deposited on SU8 epoxy after 10 min of ultrasonic cleaning suggest good adhesion and very smooth surface (WYKO NT 3300, 500x). The picture should be compared with Figures 50 and 53.

Table 5. Different SU8 formulations and coating thickness

SU8	%Solid	Kinematic viscosity (gm sec^{-1} cm^{-1}/ρ)	Thickness (μm) @ 900rpm
5	51.8	2.65	12
10	59.1	9.89	30
25	63.3	26.46	58
50	69.1	149.53	150
100	72.9	524.07	320

b. Performance of PLED on SU8

PLED devices fabricated on SU8 are of much higher quality than those previously made on other organic materials we tested so far, although they still have higher operating voltage (~7V) and lower brightness (~80% of the control device on glass at the same current density). The ITO anode on SU8 also looks reasonably clean (Figure 54). A fresh device built on SU8 showed uniform emission from the ITO electrode without marked black spots, indicating that the SU8 has a good chemical resistance to the ITO etchant and the Safestrip. Since the PLED process has not been fully optimized for this plastic material at the time of writing, we believe that the performance of PLED devices on SU8 can be further improved. Shown in Figure 55 is a comparison of a device on SU8 (right) and a control device (left) after stress test for 17 days (at 10mA/cm2).

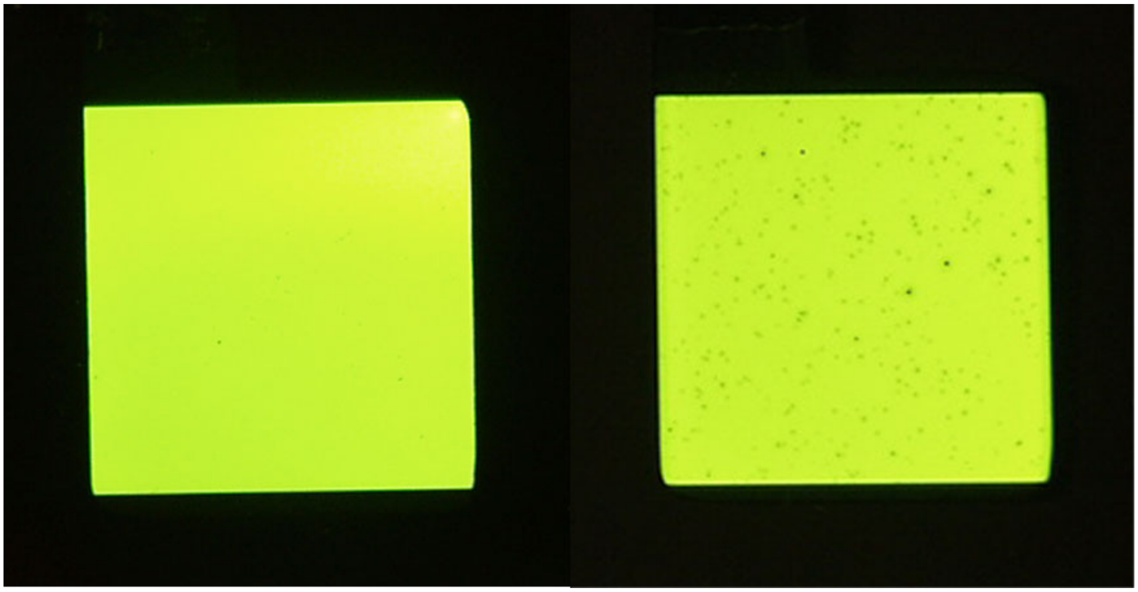


Figure 55. Shown on the left is a PLED device built on ITO/glass substrate (Applied Films); on the right is a PLED fabricated on SU8 surface (glass coated with SU8). Devices have been continuously operated at 10mA/cm2 for 17 days when pictures were taken.

The device life test also showed promising results (Figure 56). While decay rates of the device brightness are somewhat faster, and black spots developed faster in the device built on SU8 surface (though no black spots on a fresh device), the performance starts to mimic performance of devices built on ITO/glass. However, the fact that initially perfect device degrades faster is another confirmation that ITO alone cannot be used as barrier layer between the SU8 and PLED materials. We expect that upon optimizing the PLED processing conditions and introducing a proper barrier layer between the SU8 and the ITO layer, the device performance can be further improved. Therefore, we believe that it is possible to build PLED devices on SU8 of the same quality as we achieved with the regular devices built on ITO-glass.

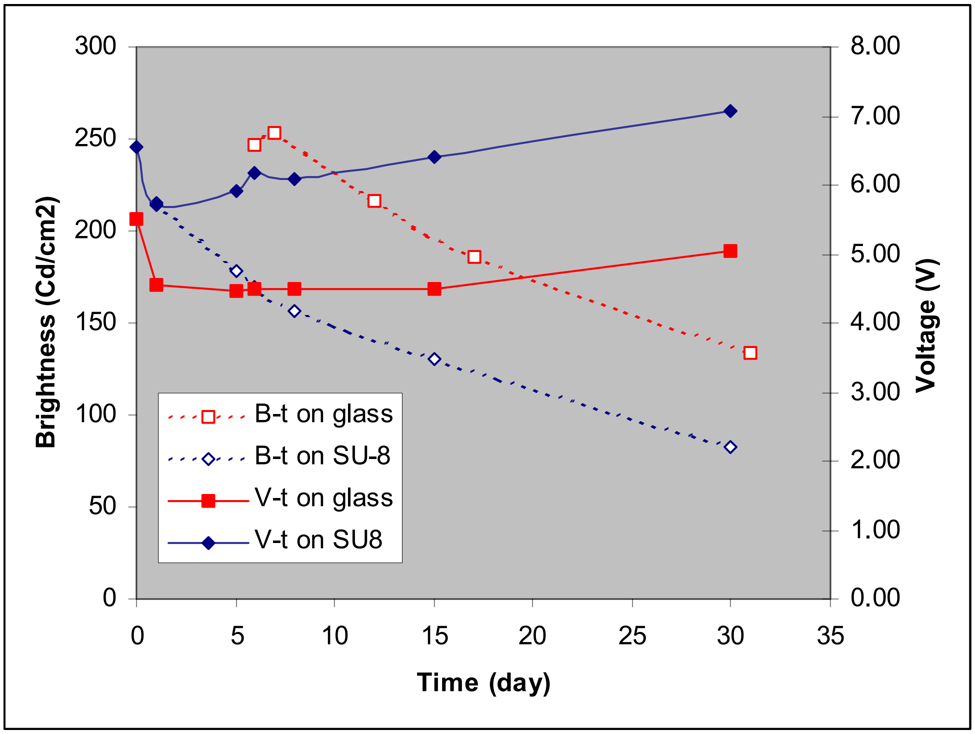


Figure 56. Degradation of PLED devices made on SU8 Epoxy and on glass.

7.3.3 Summary and Highlights

a. *ITO surface quality versus ITO deposition rate*: The rate of ITO deposition (the power level used for the sputtering process) has a significant effect on the surface smoothness of the resulted ITO film. At a lower power level (i.e. 400 W), good quality ITO film can be obtained on OG112 without wrinkles. It is therefore necessary to have the upper limit of the deposition power determined for each material in order to ensure the good quality of the ITO film to maximize production rate. Before this is done, a lower power level is always recommended for the deposition of ITO as well as other metals on these plastic materials.

b. *The post hot-press planarization anneal*: This process may not be necessary in certain cases. If it becomes necessary for any reason, it is recommended that it should be done after the spin planarization.

c. *Spin planarization*: OG112 and SU8-10 can easily planarize bumps of several μm in height to give a smooth coating. However, OG114-4, OG169, and SU8-5 are less efficient in smoothing such large bumps. It is also recommended that epoxies OG114-4 and OG169 should be degassed, and the wet coatings of these materials should not be exposed to vacuum before they are fully cured.

d. *Hot-press planarization*: Among the materials tested (OG112, OG169, OG114-4, and NOA83H), OG169 is found to be the best fit for the hot-press planarization, since it gives the smallest boundary peaks.

e. *Receptor site embossing*: UV epoxies OG114-4, OG169 and OG112 can form higher quality receptor sites than NOA83H does. When applied to glass substrates, OG114-4

has the best adhesion; OG169 is poorer than OG114-4 but better than OG112. Glass substrates should be sufficiently cleaned with O_2 (or SF_6/O_2) plasma to increase adhesion before casting.

f. *Chemical Resistance*: Based on visual inspection only, all three UV epoxies seem stable when exposed to Safestrip and IPA but can be dissolved in certain extent by acetone even when they are fully cured. These materials may not be very stable in ITO etchant (a mixture of HCl and HNO_3). In contrast, SU8 seems stable (also by visual inspection only) to all these chemicals.

g. *Adhesion of ITO to the plastics*: The adhesion of ITO to the above plastic materials decreases in the order of SU8 >> OG114-4 > OG169 > OG112 > NOA83H. ITO film deposited on SU8 can be cleaned in ultra-sonic bath without causing visible damage to the ITO film.

7.4 Optimized NB Back Plane

Based on the results described in previous chapter, we proposed the optimized structure for flexible NB backplane (dedicated for PLED displays) to make the best use of each material. The proposed backplane structure is as follows (in order of processing flow):

i) Embossing layer: OG114-4
ii) Hot-press planarization: OG169
iii) Top layer: Spun-on SU8-10

7.4.1 Preliminary Results

Shown in Figure 57 is a PLED device fabricated on top of the optimized TV-2 backplane consisting of an OG114-4 embossing layer (~100µm thick), an OG169 hot-press planarization layer (~3µm thick), and a SU8-10 (~8µm thick) spin planarization layer. When compared to the device on a single layer of SU8 (Figure 55), this device has much denser black spot population. In addition, severe cracking are observed on the SU8 layer. To improve the quality of SU8 surface, it was necessary to optimize its process parameters.

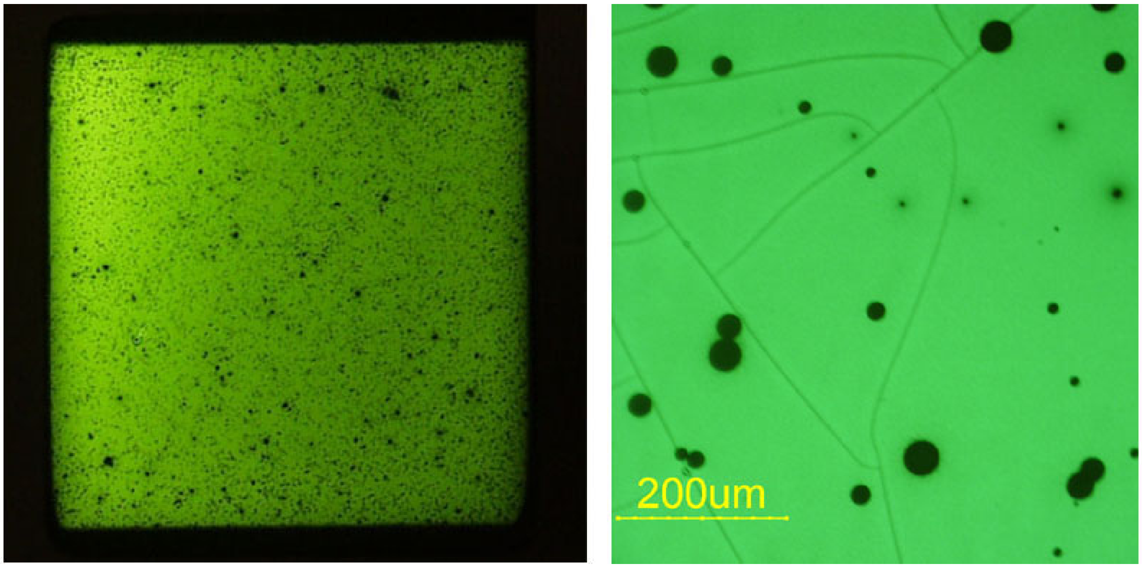


Figure 57. Shown on the left is a PLED device on TV2 substrate with OG114-4 as the embossing, OG169 as the hot-press planarization, and SU8-10 as the top layer. Shown on the right is a magnified view of the device under a microscope (100x). Device was 17 day old when pictures were taken. Operating voltage: 6V @ 10mA/cm^2.

7.4.2 Optimization of the SU8 Process

The quality of the SU8 surface is strongly affected by the processing conditions, such as exposure dose, bake temperature, etc. One of the most severe problems we have encountered during the development of the integrated NB backplane is cracked surface after processing the SU8 in the developer solution. This suggests the presence of strong tensile stress within the SU8 layer. This tendency to develop cracks after this processing step can be reduced by using altered pre-exposure and post-exposure bake conditions.

7.4.2.1 Spin-coating of SU8

The SU8 formulations suitable for spin-coating are SU8-5 and SU8-10. The viscosity of SU8-5 is comparable to those of OG114-4 and OG169 UV epoxy, while the SU8-10 has a viscosity close to OG112 UV epoxy, *i.e.*, 260 and 990 cSt, respectively. The film thickness (of the dry films) *versus* spin speed of these materials is summarized in Figure 58. It should be noted that data of Figure 58 were obtained from coatings spun on a glass substrates; when coated on plastic materials the actual thickness may slightly differ.

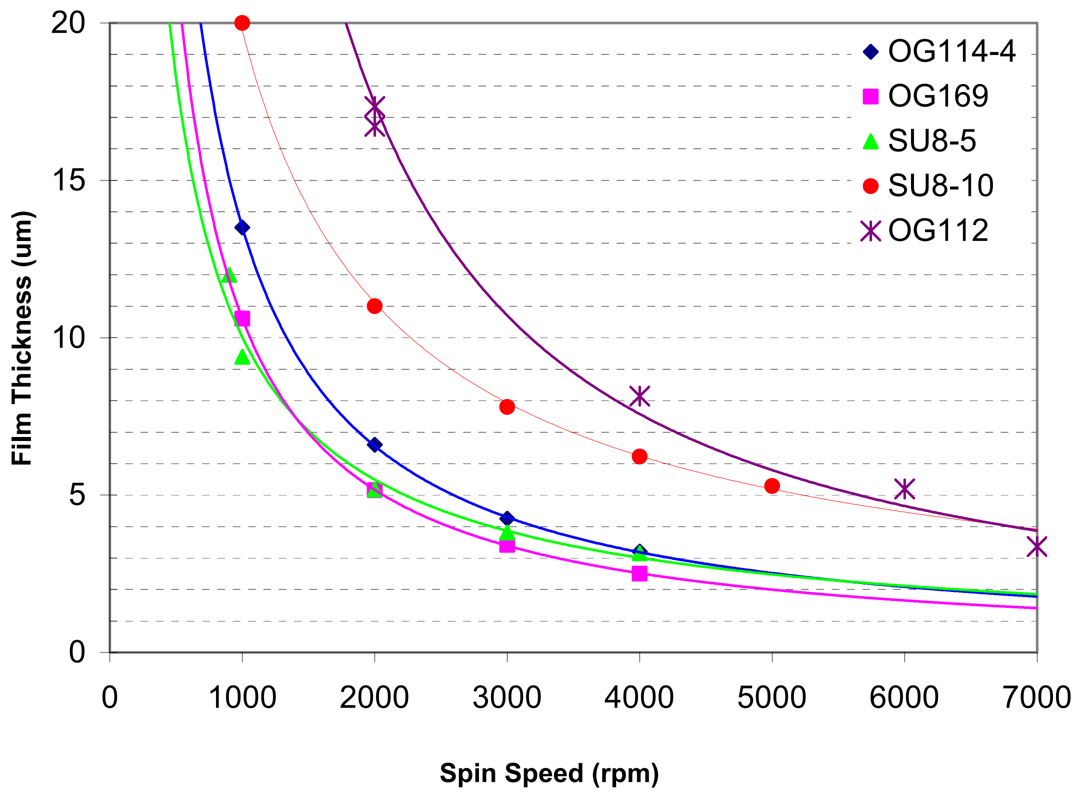


Figure 58. Spin speed versus film thickness for materials used for fabrication of the optimized NB backplane

7.4.2.2 Pre-exposure Bake

Since SU8 contains an organic solvent, it is necessary to dry the film after spin-coating. This is done by the pre-exposure bake. The manufacturer recommends to bake at temperature of 95°C, above the T_g (55°C) of un-polymerized SU8. Baking at this temperature will allow the resin to reflow, which will result in a smoother surface of the coating. Therefore, the substrate should be laid flat during the whole baking process. The following are the baking conditions recommended by the manufacturer:

a) 70°C for 3 minutes
b) 95°C for 30-40 minutes for a coating of 8-10μm thick (dry film)
c) Cool to room temperature

The purpose of step a) is to release the internal strength of the film. However, we found that the SU8 films processed using the above conditions still crack after the SU8 layer was developed (Figure 57), indicating that the internal stress was not completely relieved. The modified bake conditions performed on a programmable hotplate can significantly reduce the cracking of the SU8 layer:

a) Initial temperature of hot-plate: 45°C; ramp up to 95°C in ~10 minutes.
b) Baking at 95°C for 35 (for SU8-5) or 45 (for SU8-10) minutes.

c) Shut off hot-plate and allow substrate to cool to room temperature on the hot-plate.

These bake conditions are suitable for a dry coating thickness of 8-10μm. We experimentally verified that the SU8-10 requires ~30% longer baking time than SU8-5 for the same film thickness.

7.4.2.3 Exposure Dose

We also observed that the proper exposure dose of SU8 depends not only on the thickness of the SU8 layer but also the chemical composition of the layer beneath. For example, SU8 coated on OG114-4 requires much less UV dose then those coated on OG169 and OG112 (see below). Several levels of the UV dose were tested for an SU8 layer (~10μm thick) coated on substrates with different combination of epoxy layers.

7.4.2.4 SU8 Coated on OG169 and OG112

A substrate coated with OG169 was spun with a SU8 layer of 10μm thick. When 180mJ/cm^2 UV exposure dose was used, after it was developed, it was observed that the depth of the resulted groove is slightly less than the thickness of the SU8 layer (Figure 59, picture on the left). In addition, the bottom of the groove is somewhat rounded. This is an indication of residual SU8 at the bottom, suggesting that the resist was over exposed. In another experiment, when the SU8 layer was exposed by 120mJ/cm^2 and developed in the same conditions, the resulting groove is 10μm deep (thickness of the SU8 layer) and has a flat bottom, indicating the correct exposure (Figure 59, picture on the right). Similar observations were also made when SU8 was coated on OG112.

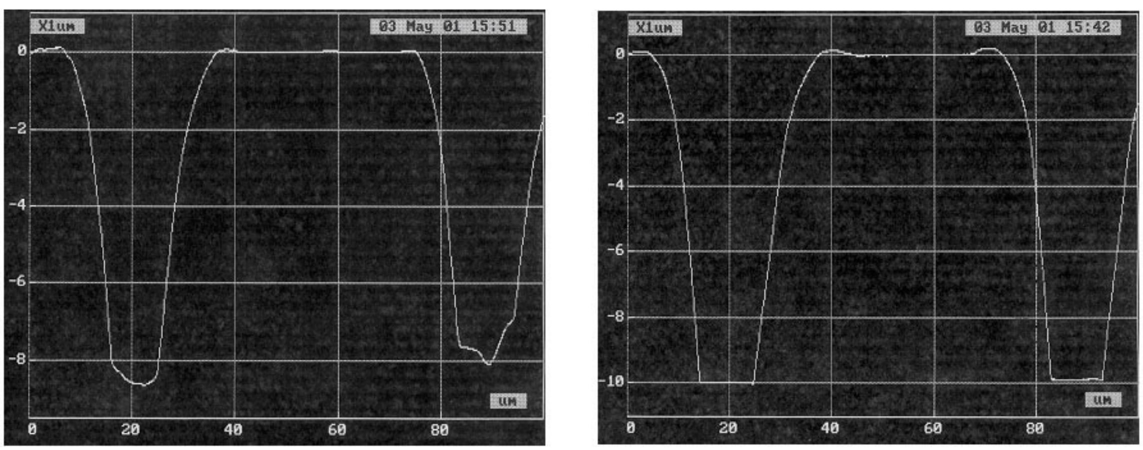


Figure 59. The developed SU8 layer (10mm thick) coated on top of OG160 exposed for 180mJ/cm2 (left) and 120mJ/cm2 (right).

7.4.2.5 SU8 Coated on OG114-4

Interestingly, when SU8 was coated on an OG114-4 layer, an UV dose of 100mJ/cm^2 appeared to cause an over exposure. After the SU8 was developed, we found that the groove depth was much shallower (only ~1.8mm, Figure 60). Longer development time does not change the groove depth. One of the possible explanations is that there is some

active specie on the OG114-4 surface, which could catalyze the SU8 polymerization. Another possibility, although not very likely, is that the refractive index mismatch at the interface of the SU8 layer and the OG114-4 layer results in a strong reflection of the UV light, which causes this over exposure. Due to the lack of time, the mechanism of this phenomenon has not been studied. As a temporary solution for this problem, we avoid using OG114-4 in direct contact with the SU8 layer.

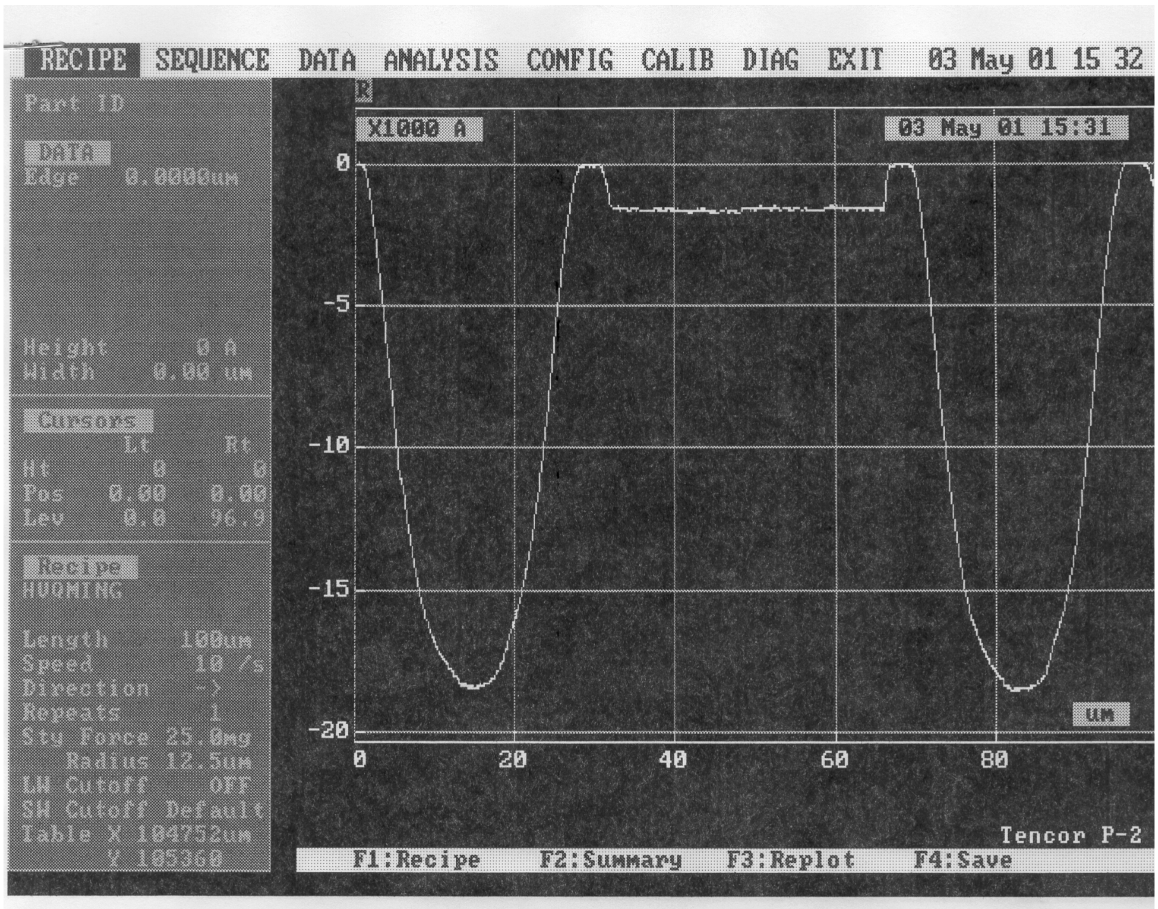


Figure 60. SU8 film (10mm) coated on OG114-4. Exposure dose = 100mJ/cm2; time of development = 3.5 minutes.

7.4.2.6 Post-exposure Bake

The manufacturer recommends a two-step bake: 95°C for 15 minutes, followed by 75°C for 3 minutes. We found that gradual heating and gradual cooling of the substrate is necessary to reduce the cracking of SU8 layer.

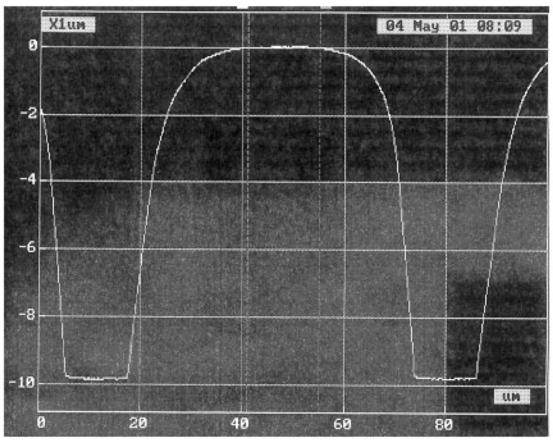
7.4.2.7 Develop

For a SU8 coating of 10μm thick and with correct exposure, it is found that 3.5 minutes development time is sufficient. However, to achieve better via yield, the developed substrates have to be rinsed with fresh developer 3 times (30 second each) to insure the com-

plete removal of any residual of SU8 from via openings. Finally, the substrates are rinsed with 2-propanol and DI water.

7.4.2.8 Post-develop Bake

The purpose of post-develop bake is to complete the polymerization and re-flow the coating surface. The chemical resistance of the SU8 layer depends predominately on the bake temperature and time. The manufacturer recommends 200°C for 15 minutes. To avoid damage to sub-layers on the substrates we are using, we elected to use 150°C for 20 minutes. It was found that baking at this condition can also further smoothen the surface (Figure 61) and provide reasonably good chemical resistance of the film.



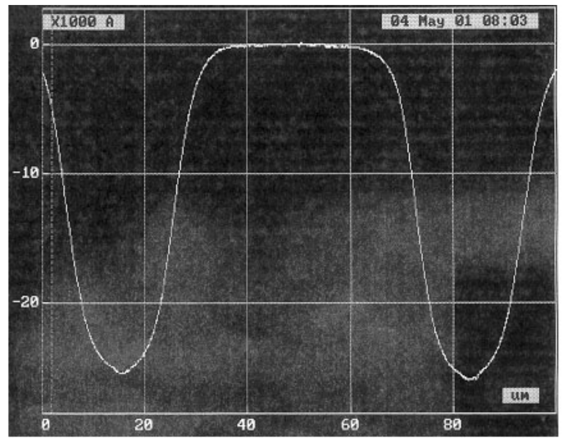


Figure 61. SU8 layer coated on OG169 (left) and on OG114-4 (right) after post-develop bake at 150°C for 20 minutes. The surface of SU8 films was smoother (featureless) after the bake - compare to Figures 59 and 60.

7.4.2.9 Drying of the Backplane

It was found that the above plastic coated substrates need to be thoroughly dried before proceeding with fabrication of PLED structure. In early experiments we observed Al cathode with black or purple discoloration near its perimeter. Also diffuse reflectance often accompanied the edge discoloration, suggesting a rough surface underneath. In addition, the thickness of the cathode was significantly smaller then that on a control sample (an ITO/glass substrate). When the substrates are baked in a vacuum oven (~90°C, ~26 inch Hg of vacuum) for a week or longer before performing the PLED fabrication process, the black edges are significantly reduced and the cathode thickness is essentially the same as that of the control sample. Similar results were achieved by baking the substrate under high vacuum (in the evaporator's load lock) for 12 hours. A comparison of devices fabricated on substrates that have been baked in a vacuum oven for overnight (picture on the left) and for a week (picture in the middle) is shown in Figure 62. These results suggest that the outgassing of the backplane materials or chemical species absorbed during wet processing is a major cause of the cathode edge discoloration and of the reduced thickness of the cathode.

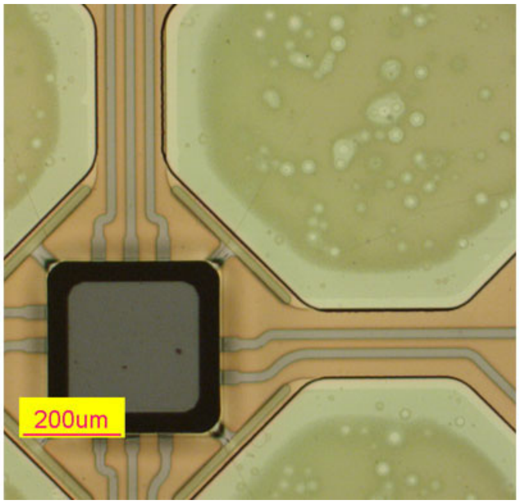
Figure 62. A view of the Ca/Al cathode of PLEDs fabricated on NB backplane with SU8 as the top layer. Left: substrate was baked in a vacuum oven for overnight before PLED processing Middle: substrate was baked for 10 days in the vacuum oven before PLED processing. Right: a 200nm SiO_2 barrier layer was deposited between SU8 and ITO.

7.4.3 SiO_2 Barrier Layer

As shown in Figure 62, the Ca/Al cathode-discoloration is fully suppressed when a SiO2 barrier layer is incorporated between the SU8 layer and the ITO layer. Shown on the right of Figure 62 is PLED device fabricated on a TV2 substrate with integrated backplane structure (Glass/OG114-4/OG169/SU8-10) and a SiO2 barrier layer (~200nm) between the SU8 and the ITO layer (the substrate was also baked in vacuum overnight before SiO2 deposition). No discoloration can be seen on the evaporated cathode of this device. The cathode of this device has normal appearance as observed on a regular PLED device fabricated on ITO/glass substrate using the Baseline Process.

When viewing from the front of the display under a microscope, defects were seen all over the displays not having the barrier layer (Figure 63, picture on the left). One of the possible explanations for the defects seen in the left device (without barrier layer) is that outgassing from the plastic layers attacked the Ca cathode. It should be noted that in both cases such defects were not seen in the areas covered by the photoresist. It is possible that these defects were caused by imperfections in the ITO layer. At this time, we could not determine the actual cause of these defects. Such defects were not observed on samples having the SiO2 barrier incorporated in the PLED structure (Figure 63, picture on the right).

Because of the significant improvements in device appearance and performance we incorporated the SiO2 barrier into our process. We consolidated all the changes described above into a new process that, for the purpose of this report, we call a Final TV-2 Process. The Final TV-2 Process is described the in the Appendix F and the schematic cross-section is shown in Figure 64. It should be noted here that most of the materials we used for fabrication the NB backplane during Phase I was chosen because of the need to keep processing temperature below 150°C. With the advent of plastic substrates with higher processing temperature the material choices will be different and possibly more common materials (such as polyimides) might be used in the future NB backplane designs.



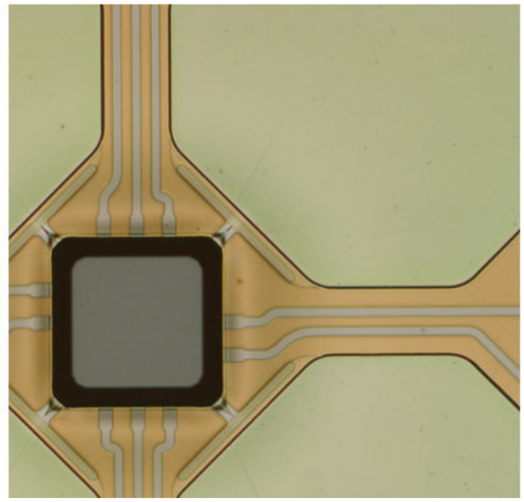


Figure 63. A Comparison of devices with and without SiO2 barrier layer: shown on the left is a partial view of several pixels in a matrix display built on integrated backplane without the SiO2 barrier layer; on the right is a partial view of several pixels without the SiO_2 barrier layer; on the right is a partial view of several pixels with SiO_2 barrier layer ~200nm thick. In both cases the back side of embedded NB IC is seen in lower left corner of the pictures.

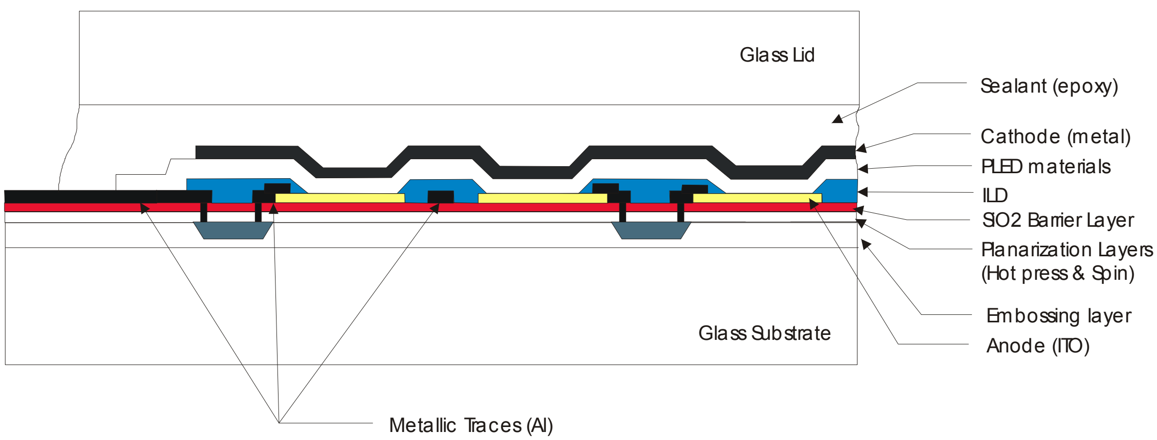


Figure 64. Schematic cross-section of the matrix TV-2 displays produced by the Final TV-2 Process

7.4.4 Device Performance

The first functional TV2 matrix displays were built on integrated backplane with a SiO_2 barrier layer (Figures 65). Although not fully operational, the functional pixels exhibit reasonable brightness (~180 cd/m^2) and operating voltage (~5.0V, the maximum output

voltage of the NB ICs). The best results from sample 1056-3B confirmed that pixel luminance of 455 cd/m^2 and external efficiency of 0.54 lm/W is possible. (the efficiency has been calculated by estimating the pixel current at 175 μA and operating voltage at 5V – those numbers represent the worst case scenario, i.e. the max values available from the Jade NanoBlock IC and the power supply).

The number of functional pixels at the time the device was first switched on is ~30%. This number increased to ~43% after the device was operated for several minutes. This phenomenon usually indicates that a number of the pixels were shorted by pinholes, which were subsequently cured by the current passing through the pinholes. Upon comparing the two pictures shown in Figure 65, it can also be concluded that most of the NB ICs are connected to ITO pixels via METAL 1. Only 14 out of total of 48 NB ICs are in doubt since all the pixels driven by these NB ICs never lit up. Further tests on TV-2 displays confirmed the above conclusions.

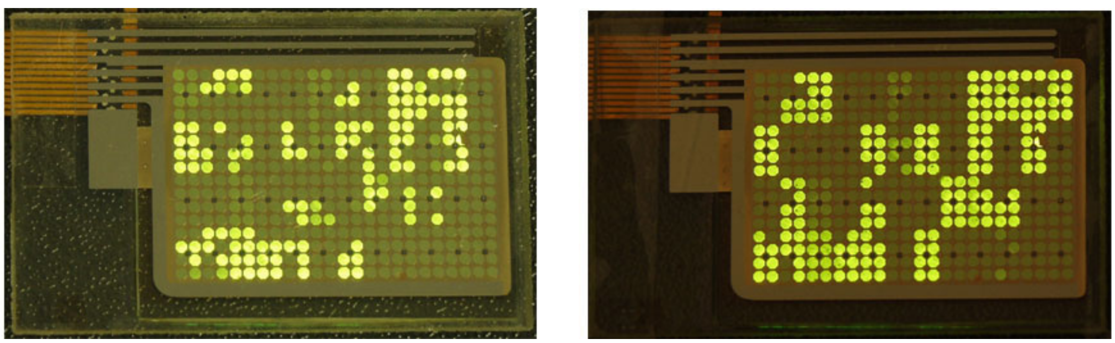


Figure 65. The first partially functional TV2 16´24 matrix display built on the integrated NB backplane with a SiO2 barrier layer. Left: fresh device; right: after aging for several minutes.

Several matrix TV-2 displays made recently show up to 80% operating pixel and further improvements are expected in the near future as we are gaining better control over critical processing steps.

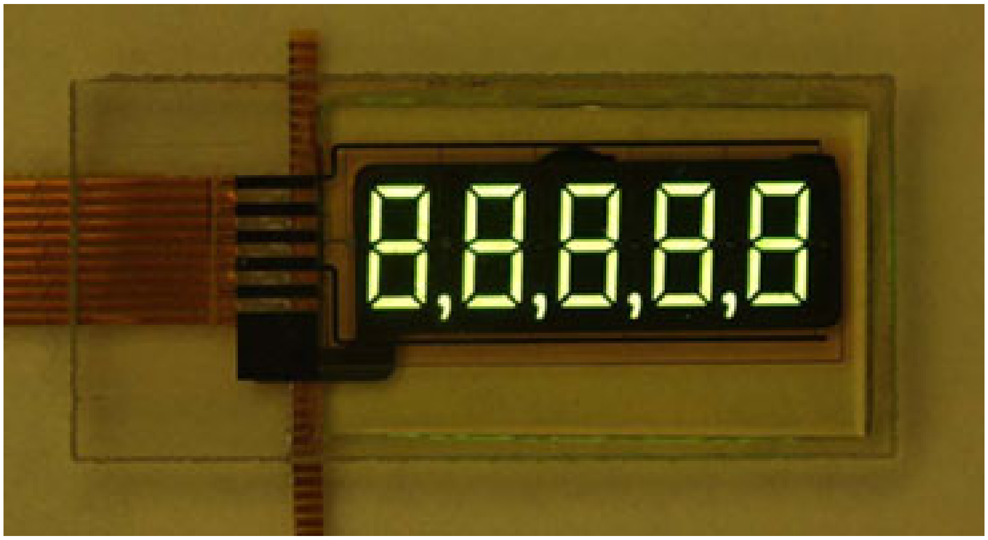


Figure 66. Fully functional segmented display exhibits acceptable uniformity (±10%) at brightness of 450 cd/m2 and external efficiency of 0.5 lm/W.

We enjoyed even better success with segmented displays, as several fully functional displays (Figure 66) were fabricated on the same TV-2 substrates. While the uniformity measurements were influenced by the presence of black spots, the measurements of brightness and power consumed by the displays confirmed that the best estimates of the brightness and efficiency stated above for the matrix displays are achieved routinely on the segmented ones. We thus conclude that we have exceeded the performance goals for Phase I set at the beginning of the program (and repeated in the Preface section of this report): luminance of 150 cd/m^2 and efficiency of 0.3 lm/W for the Green K emitter.

7.5 The "Tri-layer" Approach

As mentioned previously, it was found that the ITO surface was contaminated by an unknown organic species after the ITO patterning process. Although this situation is improved when SU8 is used as the top planarization layer (the layer in direct contact with ITO), it is still possible that the ITO patterning process produces some low-level contamination. To ensure the ITO anode not being contaminated during the process, we developed the "tri-layer" approach. In this approach, a protective Al layer is used to cover the ITO anode during the whole ITO patterning process. The protective Al layer is removed after the ITO patterning process is completed. This approach will ensure the ITO anode is not exposed to ITO etchant and to the Safestrip during the patterning process, and thus the ITO electrode should not be affected by any contaminants. A schematic illustration of this approach is shown in Figure 67. In this approach, the deposition of ITO, Mo, and Al are done together to form a three layers (ITO/Mo/Al) structure. This "tri-layer" is then patterned using a mask consisting of the overlap of the image of Al wires and the image of the ITO anode pads (the ITO/wire patterning step in Figure 65). Since all ITO pads are still covered by the Mo/Al layers after the etching process, the ITO pads will not see the organic solvent during the photoresist strip. In the following

anode-patterning step, the photoresist is patterned with mask consisting of the negative image of the ITO anodes. The ITO anodes are exposed after the protective metal layers (Mo/Al) are removed by Al etchant. Since this photoresist layer also serves as the insulating layer (ILD) of the device, the photoresist stripping is not required. We thus expect that this approach could prevent the ITO contamination caused by the use of the Safestrip.

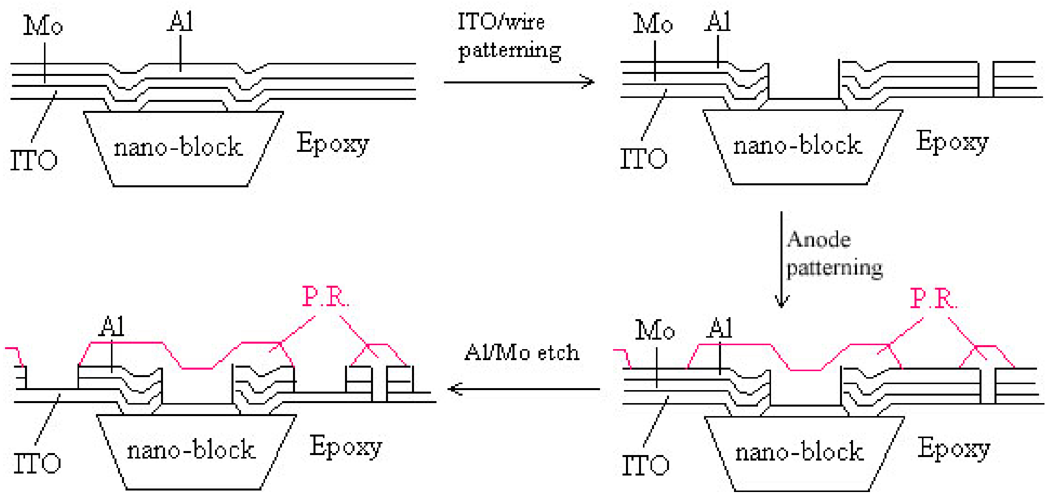


Figure 67. A schematic demonstration of the "tri-layer" approach

Another benefit of using the "tri-layer" approach is that it could prevent the damage of ITO inflicted by the sputter etch, that is used to clean the contact pads of the NB ICs prior to the metal deposition. In the Standard Manufacturing Process, an eight-minute sputter etch is used to clean the contact pads of the NB ICs before depositing the metals. Since in our initial process the ITO was deposited and patterned before this cleaning process, the ITO layer is exposed to this sputter cleaning process. It was found that the thickness and possibly the chemical composition of the ITO were changed after this sputter cleaning process. In the "tri-layer" approach, however, this sputter cleaning process is done before the ITO is deposited. Therefore the ITO is not directly affected.

Not shown in the Figure 67 is another beneficial feature of the "tri-layer" process: the metal wiring connecting NB ICs with ITO electrodes rests on the surface of hot planarization layer (OG 169), i.e., below the SU8 surface. This may prove to be of great benefit when minimizing the parasitic capacitance between the clock line and the Ca/Al cathode. Measurements on recently fabricated TV-2 matrix displays suggest that he RC constant of the clock line is large enough to deform (widen) fast pulses to the degree that makes the Jade NanoBlock ICs inoperable. Thus by increasing distance between the METAL1 and cathode can mitigate the problem.

We have just started to investigate the "tri-layer" patterning/etching process. Our preliminary results suggest that this process is feasible, though for better process control one or two photolithographic masks must be altered and the process itself needs to be optimized.

7.6 Conclusions

- We have demonstrated that it is possible to build a PLED display driven by NB IC drivers embedded into the flexible backplane.
- The optimized integrated NB backplane structure OG114-4/OG169/SU8/SiO2 is suitable for flexible PLED display.
- Pixel luminance of 455 cd/m2 and efficiency of 0.54 lm/W has been demonstrated on matrix display with Green K polymer.
- At least one barrier layer needs to be inserted between the SU8 layer and the ITO anode in order to assure fully functional PLED display.
- The "tri-layer" approach seems to be the best solution for preventing the anode from contamination and for reduction of parasitic capacitance of the clock line.

8. WEB PROCESS DEVELOPMENT

Over the past year, we have started to experiment with for roll-to-roll coating of the PEDOT and LEP layers onto smooth plastic films. The primary interest was to replace the standard spin casting of the PEDOT and LEP with technology suitable for web processing. One of such techniques has already been proven by the pioneering work of Seiko Epson – the inkjet printing of color PLED displays. While the inkjet printing produced high quality color PLED display, the technology is cumbersome for producing of monochrome displays. We attempted to discover techniques which do not require such demanding surface preparation as the inkjet technique, yet would be able to produce the thin layers of PEDOT and LEP with required uniformity and morphology.

The approach of choice was to explore the coating techniques of interest by running trial coating runs at the vendor sites during the Phase I. After a thorough review of already established printing and/or coating techniques we became interested in slot die and offset gravure technologies. The slot die technique has the ability to coat thin layers without physical contact at fairly low operating speeds suitable for PLED processing. Similarly, because of its ability to induce a shear during the coating process, a roll coating technique, offset gravure, has also been included in the study.

8.1 Sheet Slot Coating

As a way of evaluating slot die coating with working PLED devices, we used a sheet slot die coating system, as all backplane development is currently limited to sheet processing. The sheet coating process can be scaled up fairly easily to web coating with the same slot die technology. Three companies were identified that make sheet coaters in the U.S.; FAS Technologies (FAS), Liberty Coating Systems (Liberty), and Frontier Technology Inc.(Frontier). FAS and Liberty had working units in-house, and both were evaluated. The Liberty unit could not produce repeatable results and no clean room was available. The FAS unit was used on two occasions for experimental coatings with very repeatable results.

8.1.1 Liberty Precision Overview

Liberty Precision Industries, Rochester, NY is a high precision machine shop that tried to market its coating dies as a separate business venture. The coating venture has recently been spun off, and is now the “Liberty Coating Equipment” arm of Coating and Converting Resources Inc. based in Sussex, Wisconsin.

8.1.1.1 Liberty Equipment Summary

- <u>Equipment Description</u>: 6” [152.4 mm] slot die deckled to 4” coating width, 0.005” [127 μm] shim, Lip estimated to be 30 mils wide.

  Die was attached to end of an ADEPT robot arm with 3D movement capability. (up/down, X/Y planar movement). Movement in X direction only required precise movement of two arms with an elbow joint.

IVEK computer controlled pumping system: This is a piston system that reset itself after every coating patch. The system can set the volume dispensed and rate dispensed.

A vacuum table held the 6”x 6” [152.4 mm x 152.4 mm] glass plates.

- The setup was at the end of a large room containing multiple operational machine tools. Some dust was visible in the air.

- Mechanical Summary: Die to substrate gap was hard to set since there was no way to adjust side to side variation other than with shim stock. In the course of the day, this was reset 3 times. This is considered to be more than normal adjustment.

8.1.1.2 Liberty Experimental

We attempted to coat Bayer BaytronP Solution with a coating gaps from 25 to 120 microns. We coated at speeds from 6.7 to 13.4 feet/min [2.0 to 4.1 m/min] and attempted wet coating thickness from 4.9 to 25.4 μm. A hand held corona tool was used to treat the glass prior to coating on some occasions. See appendix for a complete test summary.

8.1.1.3 Liberty Results

It would appear that the first coating had much smaller gaps. There is obviously a deficiency in the positioning system. As the die moved the 6 inches there was observable shuddering (twisting movement around the z axis) of the actual die. It appeared to be hitting the substrate, but that should not have been the case. The speed did not have an impact on the steadiness of the die head, and coating quality suffered some at the higher speed.

Corona treatment of the surface improved the mottle quality of the coating. We treated the surface for 45 seconds using a hand held probe.

Drying definitely played a part in the final appearance of the coating. Uneven drying, or too fast drying ruined the overall appearance. We dried acceptably by putting 12 mm plastic offset between the hot plate and the four corners of the glass slide. The hot plate temperature varied between 90 and 210°C. The final reading was 128°C.

It was recognized that the pumping system was not optimized for the coating. We came close to eliminating the initial heavy starting edge, but were not able to narrow the starting edge window to under 6 mm. This could be improved with better mechanical tolerances. Several attempts were made to clean up the trailing edge of the coating patch. A combination of stopping the flow and raising the die was not enough. A method of pulling the material back into the die will be necessary.

Repellancies were in much evidence at wet coat weights of 10 μm and under. Only a few repellancies were present at coat weights of 20 μm and above. There was visible non-uniformity in the cross web direction (TD). This is usually a result of imperfections in-

side the die cavity. In our case it could also have been a lack of sufficient pressure across the land area of the die. From initial measurements using the TENCOR profilometer, we saw variations over 35% in TD direction. Variation in the machine direction (MD) appears to be in the 10-20% range. Even at this low coating thickness, the low viscosity will allow the fluid to flow as it is being handled and moved from the die coating area to the hot plate.

8.1.1.4 Liberty Conclusions

The trial provided key insights into the difficulties we have ahead of us. Liberty is a very capable coating die company, but the experimental die we used attached to the robot arm was incapable of providing the precision required.

8.1.2 FAS Overview

FAS Technologies was founded to make precision metering systems for the semiconductor industry in 1988. Shortly thereafter, they developed an interest in the application of slot die coating to the wafer flat panel display industry. They hold more than 20 patents around between the two concepts.

8.1.2.1 FAS Equipment Summary

- Equipment Description: 180 mm slot die, 0.0015” [38.1 μm] shim, Lip Width: 0.020” [0.508 mm].
  Glass affixed to a moving vacuum table. Table is affixed to a precision ground granite table via air bearing. A linear motor moves the fixture. A glass linear positioning system provides feedback. The vacuum table is leveled at one end of the granite table. Three micrometers come down, and three servomotors adjust. One motor has just linear motion and provides physical attachment to the table, while the other two have angled slides for more refined movement. Leveling is done before every coating sample. After leveling, the sample is transported to the coating station.

- The slot die hangs above the moving sample with automated rotational movement only. Leveling of the die is accomplished manually with two fine thread adjustment screws (Duff-Norton). The normal lip for low viscosity fluid is 0.008” [200 μm] with a 45 degree angle. Between coatings, the die would normally sit in a wetting fluid to prevent skinning of the coating material on the die lips. A wiping station to clean the lips prior to coating is also normal prior to coating. A 0.0015” [38 μm] mil shim was used to separate the die lips, and they report they can go to 0.001” [25.4 μm].

- Metering of the coating media to the die was performed via their in-house developed two-stage diaphragm pump. A round piston is pushed into an oil reservoir by a servomotor. The oil then accurately pushes a diaphragm that displaces the same amount of coating fluid. With the ability to reverse, we suspect no check valves are used as in normal diaphragm pumps. The pump head has small Teflon sole

noid valves on each pump entry/exit point. This pump technology has been licensed to Millipore and represents the first FAS commercial offering. No filtration was used in our trial, and at several points during the trial, long filament elements were extruded from the die. The source of the defect has not been determined, but the first assumption is that it was present in our solution.

- Drying was accomplished on two hot plates set at 60°C. Plates were laid directly onto the hot plates.

- Coating was done in a "Class 100" clean room with lax gowning regulations. Masks were not worn over the mouth, hairnets and booties were worn, but clean room hoods and boots were not worn.

- Mechanical Summary: FAS has done everything right to fine tune mechanical accuracy and provide repeatable highly accurate movement. They report better than ±3 μm position repeatability, and we suspect twice that (±6 μm) on the system we ran. The die still had to be manually leveled and gap manually measured. With shim stock, one has to be really diligent to get within 5 μm of desired position on an absolute basis. 10 microns is probably more typical. Their new system has a fixed substrate and moveable dies. They use Keyance lasers to measure the gap distance and adjust to any variation in substrate height as they move. But even these are manually calibrated.

- Fluid Flow Summary: Their pumping system provided microprocessor control and PLC flexibility. It could pump into or withdraw from the die. It could also recirculate through the pump or a point closer to the die.

8.1.2.2 PEDOT Experimental at FAS

The first trial was set up to evaluate FAS Technologies slot die coating system in depositing thin liquid layers onto flat substrates in a 200 mm x 250mm patch format.

Coating Fluids:

- AGFA Orgacon , 0.8-1.0% solids, 25 dyne surface tension, 4 cps
- Bayer BaytronP, 1.0-1.3% solids, 68 dyne surface tension, 5 cps,

The program was to produce samples at 4 coat weights ranging from 8 microns to 40 microns in wet coating thickness. A single speed of 12 mm/sec (2.4 fpm) was used. The substrate to die gap was adjusted per desired wet coat weight to be from 4 to 9 times the wet thickness. The uniformity of the bulk coating layer, and side, leading and trailing edges would be evaluated.

Orgacon, an Agfa Gevaert product, is similar to Baytron, but has been modified by some means to increase conductivity and modified with surfactant to lower the surface tension. We included the Orgacon in our tests to study the impact of surface tension on the coating process.

8.1.2.3 FAS PEDOT Results

From an optical viewpoint, the Orgacon coatings were very uniform. In respect to fluids, the surface tension of the Orgacon allows it to cover a variety of surface imperfections. The Tencor measurements show a uniformity values from 6 to 26%. Measurement error (on the order of 15 nm) plays a large part in these numbers. Some of the error was also induced in having to manually move the samples from the coating chuck to the hot plates. Hitting the desired coat weight also proved to be difficult. Delta between calculated and measured coat weights range from 1% to 60%. There is no logical explanation for this large delta at this time. However, the system is well designed for accurate repeatability, and an explanation may be found with additional experiments.

It was determined that surface of the two sides of the glass sheets were different, as repellencies would form on one side but not the other. It would be useful in future trials to uniformly clean the glass surfaces to be coated on.

With the Baytron, the material was coated very uniformly, but surface energy non-uniformities distorted the final dry coating uniformity. An acetone wash of the glass surface allowed the Baytron not to form any repellency dots, but the wipes of the cloth used for the wiping were visible. It would appear that we could achieve a uniform coating with the Baytron in its current state only with perfect surface preparation.

The side edges were fairly uniform with a noticeable heavy bead. This bead can be minimized some with shim design, and moving the die closer to the substrate. A 2 mm bead border looks very promising. If the heavy edge proves to be an ongoing issue, bead removal can be accomplished through a variety of means (vacuum, wiping, etc.).

The leading edge was established without a heavy bead, and again it is believed that a 2 mm start border could be maintained. The coating bead was primed by leaving the die stationary at the start of the coating for 1 to 2 seconds with the pump on. There are many parameters to adjust to optimize this edge that include: pre-start time of pump, stationary time, and height of die during bead initiation, acceleration rate of platform. Our edge looked acceptable without major optimization.

The trailing edge optimization did not go smoothly. All samples for except for the thinnest coatings had a very heavy edge that then leveled back into the coating 10-20 mm. The parameters to adjust are similar to the leading edge parameters: die height acceleration, die height velocity, pre-shutdown time of the pump, pump suction rate and time. The technician at FAS was very wary of using the suck back ability of the pump. He believed that this method is often not necessary and is time consuming to optimize. The concern is that one does not bring air back into the die cavity. With enough time on the equipment, this issue could possibly be overcome.

8.1.2.4 FAS PEDOT Conclusions

It was shown that the system can achieve the coating uniformity that we require. FAS claims to be able to maintain ± 1.5% thickness uniformity with coatings with wet thickness greater than 25 μm. This spec becomes more difficult with the thinner coatings. We

achieved respectable ± 6% with a 15 μm wet thickness in our first trial The substrate-to-die gap used in the experiment was quite remarkable. While this gap typically runs between two to four times the wet thickness, we apparently coated in the range of four to nine times the wet thickness. The increased gap is a result of the vertical position of the die. Even at the slow speeds used, this would not have been possible with a horizontal die.

With effort, it should be feasible to generate only a 2 mm zone of non-uniformity on all edges. The trailing edge will be the biggest challenge. The patch size can be controlled length wise with the pump and the motor.

The results of the first test have shown the FAS implementation of 0.008" [0.2 mm] die lips matches the thinnest in the industry. The issue around achieving the desired coat weights is troubling. The pumping system is capable of much greater accuracy and we can only presume that something is broken. Running a pump calibration check before the next trial should help determine a possible cause.

FAS has a very capable and well staffed engineering organization, and they are capable of delivering a product to meet our required specifications. The asking price of $250,000 for their small wafer coating device is expensive, but in-line with the industry standards considering the amount of engineering that has gone into its design.

8.1.2.5 LEP Experimental at FAS

A second coating trial was set up to coat LEP polymer solution onto bare glass and TV-1 backplanes.

- Equipment Setup:
- Slot Die Setup: 180 mm slot die, 1.5 mil [38 μm] shim, Lip Width: 0.007" [178 μm]
  Die velocity: 12 mm/sec, Die Acceleration: 12 mm/sec^2
  Pre-pump Time: 5 seconds, Initial Bead Pump Time: 2 seconds
  Total Pump On-time per Pass: 18 seconds, Movement time: 20 seconds
  Filtration: None
  Substrates: 200 mm x 250 mm glass plates, 6"x6" [152.4 mm x 152.4 mm] glass plates, 4"x4" [101.6 mm x101.6 mm] TV-1 backplanes
- Coating Fluid:: 1% DOW Green LEP in xylenes

A piece of 0.004" [0.1 mm] PET with a hole cut out of the middle was used under TV-1 substrates to affix the plates to the vacuum table. The die gap was setup using 200 mm x 250 mm plate of glass with the same sheet of PET underneath. All 200 mm x 250 mm glass pieces were scrubbed with detergent, water rinsed, IPA rinsed, and Nitrogen dried. They were shipped sandwiched between pieces of clean room paper. The 6"x6" [152.4 mm x 152.4 mm] glass substrates were cleaned in an identical fashion with the addition of an acetone rinse after the water rinse. The substrates were successfully shipped in plastic carrying cases. The Orgacon was applied with the Sheen coater, and the Baytron was spun on.

Drying was accomplished on two hot plates. The glass substrates would rest on 12 mm offsets on the first hotplate set at 60°C until visible moisture disappeared. Substrates were then moved to a second hot plate set at 130°C for a minimum of 10 minutes. The substrates were in direct contact with the hot plate.

The experimental program had two thrusts. The first and main thrust was to confirm that the slot die coating process could successfully produce working displays. The second thrust was to start exploring the coating operability window. See attached table for a run down of the individual trials.

8.1.2.6 FAS LEP Results
We can report success on the efforts to make four TV-1 light producing backplanes that were coated at FAS with the LEP material and completed at the Alien laboratory. The internal efficiency of the devices was measured in the range of 0.85 to 2.37 Cd/A. This efficiency is slightly lower to those produced via the current standard TV-1 spin coating process (typically in the 2.5-3.0 Cd/A range). This result was expected based on public disclosures from other companies' experiences when the LEP polymer was applied with methods different from spin coating. See Figure 68 for the typical I-V curve for the devices made with slot die compared with a typical I-V curve form spin-coated device.

It was again demonstrated that proper drying technique is key for uniform coatings after the uniform application of fluid. If left to sit on the vacuum table, the ridges in the vacuum table would represent themselves into the coating appearance. The increased heat transfer at the points the table touched the glass is the culprit. It was important to quickly remove all the substrates from the table and transport to the hot plate with the ½" offsets. This provided a uniform heat to the glass. It should be noted during the transfer of most of the coatings, one could see the drying line creeping in from the edge during the transfer. On very thin coating, the drying line had reached the center point before the plate reached the hot plate.

For the majority of coatings, the coating uniformity was visually excellent after the initial coating. The drying line always proceeded from the edges to the center. On the thicker coating, the ridges developed during the drying became permanently visible. On the thin coating, the lines were barely visible. Coating thickness was measured using the Tencor profilometer. With the noise level involved, the accuracy of the measurements is estimated to be ± 5.0 nm. This noise is typically 10% of the actual thickness.

With the TV-1 structures, even more non-uniformities become apparent. W01212A, with 110 nm thick coating, is the only sample with small streaks in line with the die movement (Figure 69). This would normally occur if the die gap is too narrow. The three TV-1 structures with lower coat weight show the LEP thickness increasing from the start to the finish with thickness variations flow patterns perpendicular to the die direction. Figures 70 and 71 show two of the other TV-1 devices made from this run.

The measured coated weight data indicate that there is a significant transition period as the die starts coating. On this test, the data shows an increasing coating weight at the die

moves. Optimization of the starting conditions can improve this, but is a painstaking task. The average data also shows a skew between the left and right sides. This is not surprising, as the die was not level when rechecked at the end of the trial.

The material coated well over the three different surfaces: bare clean glass, Orgacon, and Baytron. The etched ITO structures on the TV-1 substrates did not cause any coating disturbances that were visible with our inspection techniques.

One series was attempted to determine the maximum coating gap. We achieved coating with an estimated 7 mil gap, but lost coating with a 9 mil gap. This correlates to over 20:1 gap to wet film thickness ratio. On a high speed coating line, this ratio is typically 2 to 3.

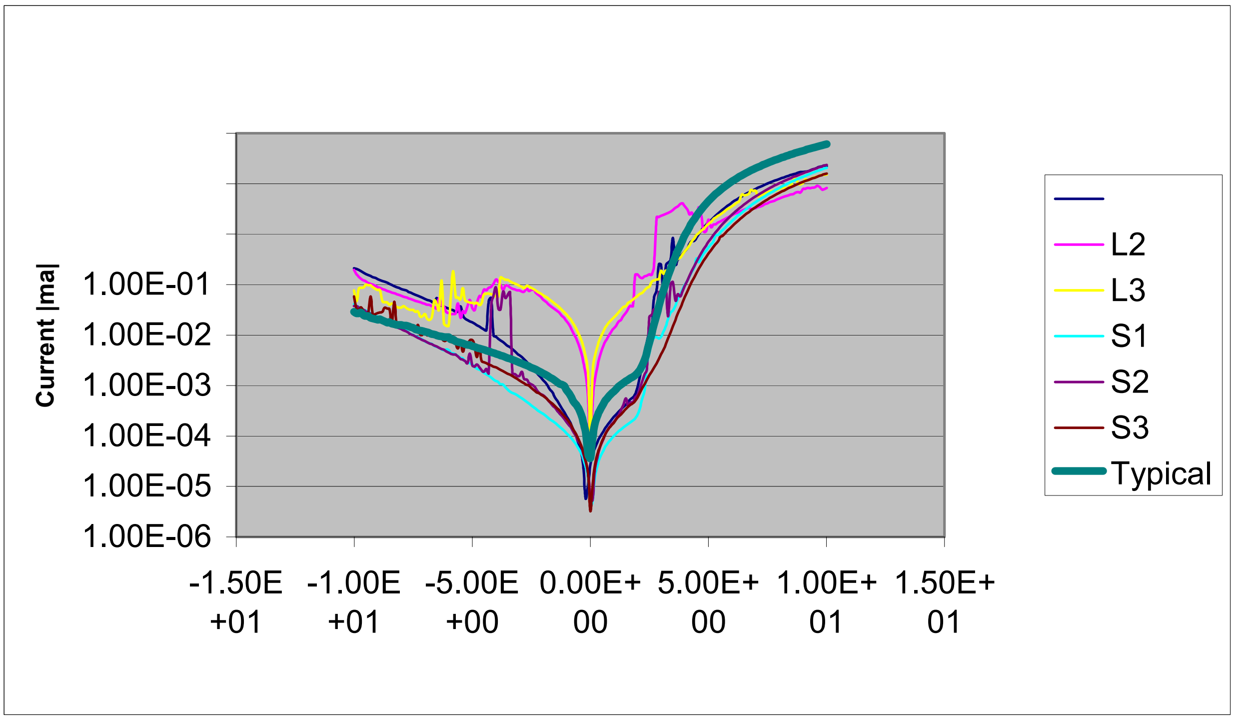


Figure 68. Comparison of I-V curves of devices produced by slot die coating with devices produced by spinning.

Another series of tests attempted to define the minimum wet thickness that could be put down. We achieved a dry thickness of 34 nm at the minimum pump speed of 2 μl per second. In theory, this should result in a dry thickness of 7.5 nm. The difference cannot be easily explained, but pump calibration would have to be checked first before drawing any conclusions. It seems that 34nm thickness is very close to the minimum thickness achievable with the 1% LEP solution and the slot die system.

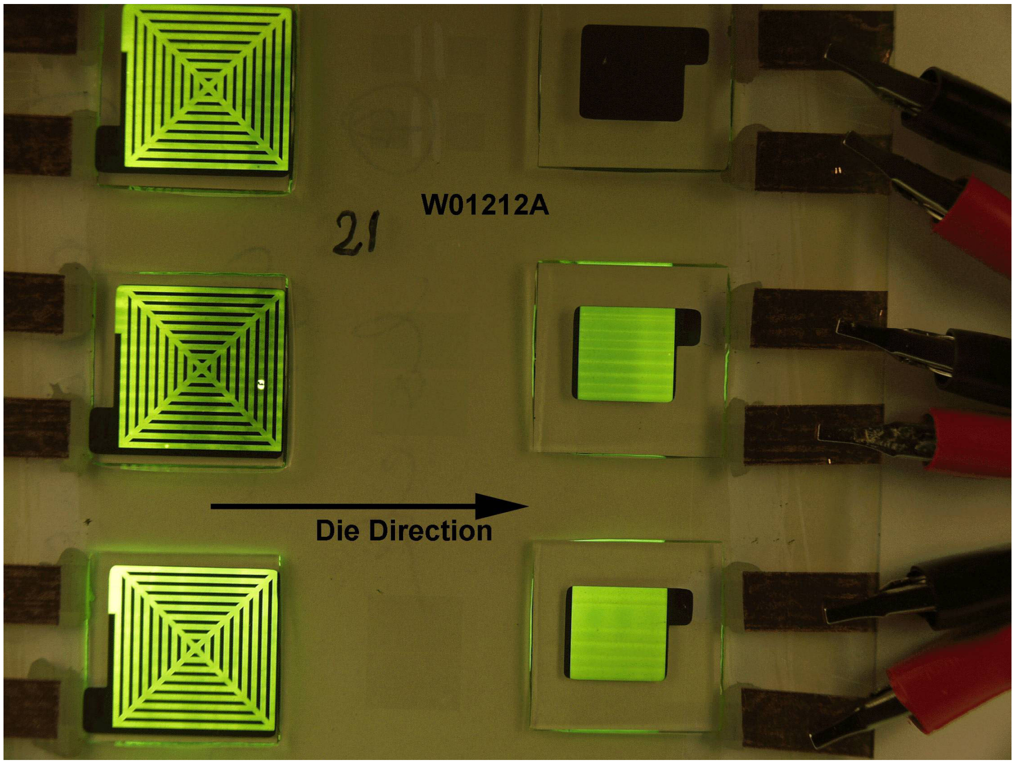


Figure 69. TV-1 device W01212A, showing streak coating non-uniformities.

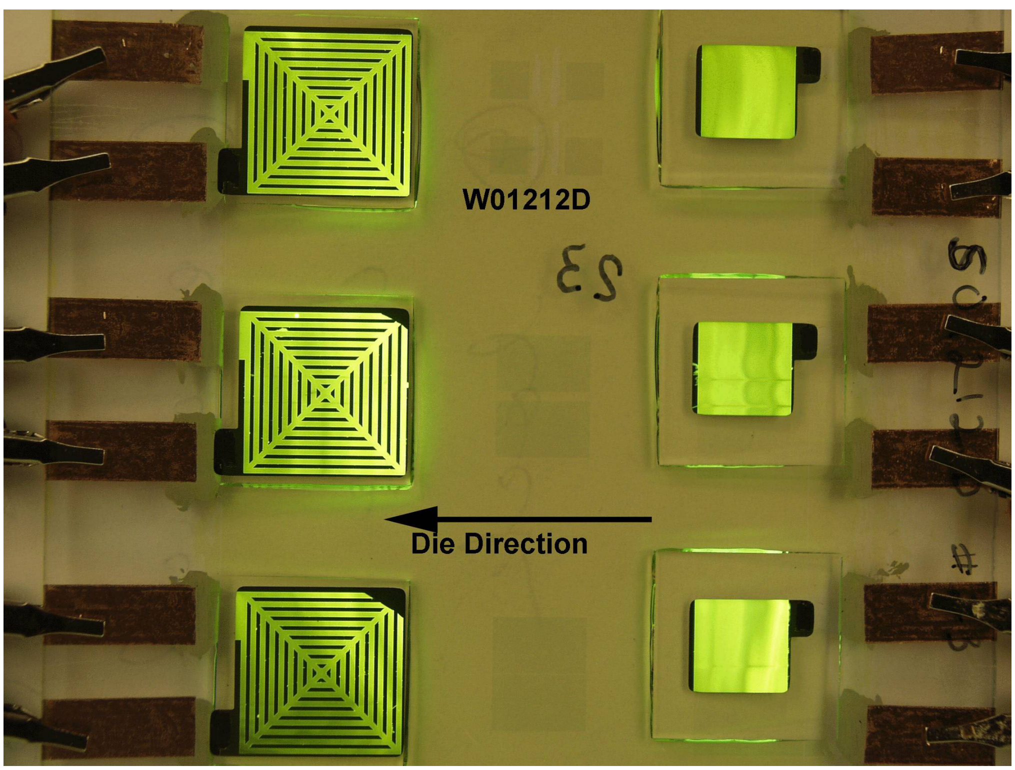


Figure 70. TV-1 device W01212D, showing coating non-uniformities.

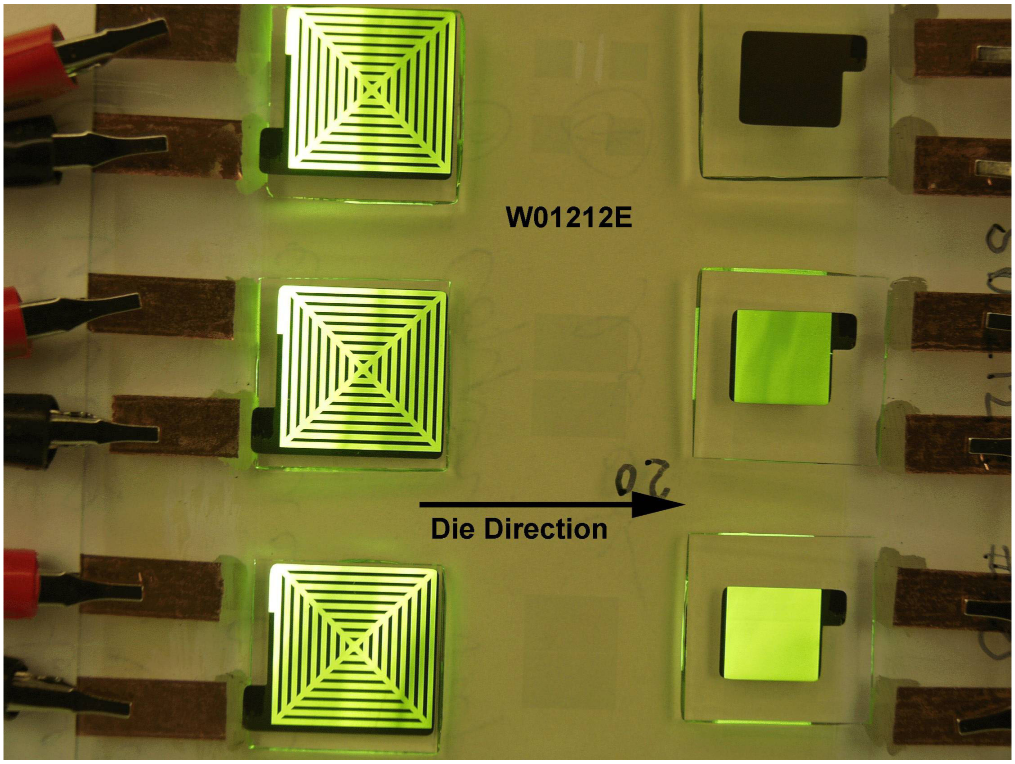


Figure 71 TV-1 device W01212E, showing coating non-uniformities.

8.1.2.7 FAS LEP Conclusions

This initial trial with LEP polymer (DOW green) gives the slot coating method viability for producing monochrome PLED devices on a web line. The luminescence measured was lower than spin coated devices, but no process optimization was attempted during this trial. From a process standpoint, the drying method and profile have the best potential to improve luminescence efficiency, but improvements will also need to be looked for elsewhere (such as formulation, coating method, coating parameters, etc.)

There were no process issues for coating the LEP polymer with a slot die. The solution provided excellent quality coatings over all surfaces attempted. The low viscosity makes post-coating flows an issue, but properly designed equipment should be able to overcome them.

8.1.2.8 Path Forward

The technology has been proven out to be capable of making working devices. The next step would be to acquire appropriate funding to purchase an in-house coater for continued development work, or to work with a coating partner to optimize the process. Integration with Alien Technology NanoBlock IC backplanes into a slot-coated PLED system could be important for the construction of displays or other “smart” devices.

8.2 Web Slot Coating

While there are various facilities to coat at across the country, Frontier Industrial Technology (Towanda, PA) was chosen for its size, coating expertise, and cost factors. As with sheet coating we demonstrated that slot coating can be used to coating the PEDOT and LEP coatings and produce working devices.

8.2.1 Frontier Overview

A standard single cavity slot die was used with longer than normal land area (about 1.5”or 38 mm). Frontier maintains the longer land helps the uniformity with thinner coatings. This is true, but it also increases the critical area for precision machining. The lip faces were 0.015” [381 µm], and they expect to go to 0.010” [254 µm] for their next set. A 0.005” [µm] plastic shim was used between the lip faces. The shim was cut to give a 0.5” [12.7 mm] striped coating pattern. The die was angled up 15 degrees, but the contact angle on the substrate was 90 degrees. They have used other contact angles by adjusting the die support bracket, which is a slightly expensive proposition, and have also offset the die lips for some test work. Offset die lips refers to the practice of having one die lip jut beyond the plane of the lower or upper die lie lip by a few thousands of inch.

A vacuum box was used to help stabilize the bead and increase coating gaps. 250 Pa pressure was typically used. Air cylinders were used to move the die in and out against hardened stops. For quick in/out movements, the die was pulled out by hand. The movement of a fine-pitched screw adjusted the die gap. A wheel provided approximately 50 clicks per revolution. One click represented a change of 0.0002 mils [5.1 µm]. Also present in the lab was a dual slot coating head. The die had an internal combination of the fluids. They are currently working with PCI (Precision Component Industries) on the fabrication of the single and dual slot coating heads. PCI has a very good reputation in the coating industry.

The pumping systems consisted of a simple Cole-Parmer gear pump with a digital flow control display. There were no actual flow feedback loops. Tygon tubing was used for all the fluid lines, indicating very little pressure present in the die. A manual three-way valve directed flow to the die or into a recirculation loop. A unique 20 ft [6.1 m] one zone dryer was used. The film was floated over an arched perforated metal plate. The gap between the plate and the floating film was a function of air pressure and web tension. The stability of the web appeared to be acceptable. Impingement nozzles on a 3” [76.2 mm] pitch blew air down onto the coated surface. The impingement nozzles could be moved up and down or pitched from front to back of the zone. A rubber roll facilitated a turn around and the web came back with the impingement nozzles now blowing up from the bottom. The coated side of the web makes contact with a rubber roll at the end of the dryer and then proceeds to the windup. Airflow was adjusted with variable speed fans, with one fan for the nozzles and another for the central perforated plate. Heat was generated with electric resistance heaters.

8.2.1.1 Stripe Coating Experimental

An aqueous polyvinylalcohol (PVA) polymer solution of approximately 10% concentration was used to demonstrate the coating operation. Parameters for the first phase of the trial:
Viscosity: 68 cps (68% @ 6 rpm w/ Brookfield UL adapter)
Line speed: 5 fpm [1.5m/min]
Flow Rate: 8 ml/min
Die to web Gap: 4mil [100 μm] estimated
Vacuum Pressure: 200 Pa
In the second phase, the PVA solution was diluted with water to a viscosity of 13 cps (65% @ 30 rpm w/ Brookfield UL adapter)

The goal of the experiment was to demonstrate stable coating of 12 half-inch [12.7 mm] stripes with half-inch [12.7 mm] spacing. With the pump set at the minimum flow rate, the wet coating thickness was roughly 35 μm. The stripes were very stable with when the coating gap and vacuum were adjusted appropriately. The stripe width averaged 13 mm for the higher viscosity material, and 17 mm for the lower viscosity material. There was also more variation of the stripe width from one side of the die to other for the low viscosity material. It was observed that the coating gap played an important role in the stripe width. As the die was brought closer to the web, the bands tended to spread out more. It was possible to coat a continuous sheet with no bands when the gap was small enough. The die shim was not optimized for either viscosity, but was probably especially big for the low viscosity material.

For creating patches, three avenues were pursued. The first approach was to just pull the die out and back in without stopping the flow. This resulted in a thick back edge and a thick starting edge, but both edges were fairly square if the movement was fairly quick (refer to Figure 72). The second method attempted was to just stop and start the fluid flow. This produced long tapering trailing edges and rounded starting edges. A combination of the two techniques was tried with limited success (refer to Figure 74). Several starts and stops with close to square corners were produced, but repeatability was not present. A 4 mm wide trailing edge non-uniformity was common throughout the test. If this non-uniformity is to be reduced, the ability to suck material back into the die cavity will be necessary. The leading edge took a minimum of 30 mm to reestablish its steady state parameters in this primitive exercise.

Automation of the die and valve would likely reduce some of the length, and slowing the line speed would also help. The largest portion of the transition is possibly caused by the reestablishment of the vacuum pressure as the die is put back in place. At the run speed (25 mm/sec), this time transition time is approximately 1 second. One way around the problem is to reduce the coating gap to the point that a vacuum box becomes unnecessary. Another, more difficult way is the idea of bringing the coating fluid back into the die without retracting the die, thus maintaining the vacuum pressure. This sounds too problematic to pursue further.

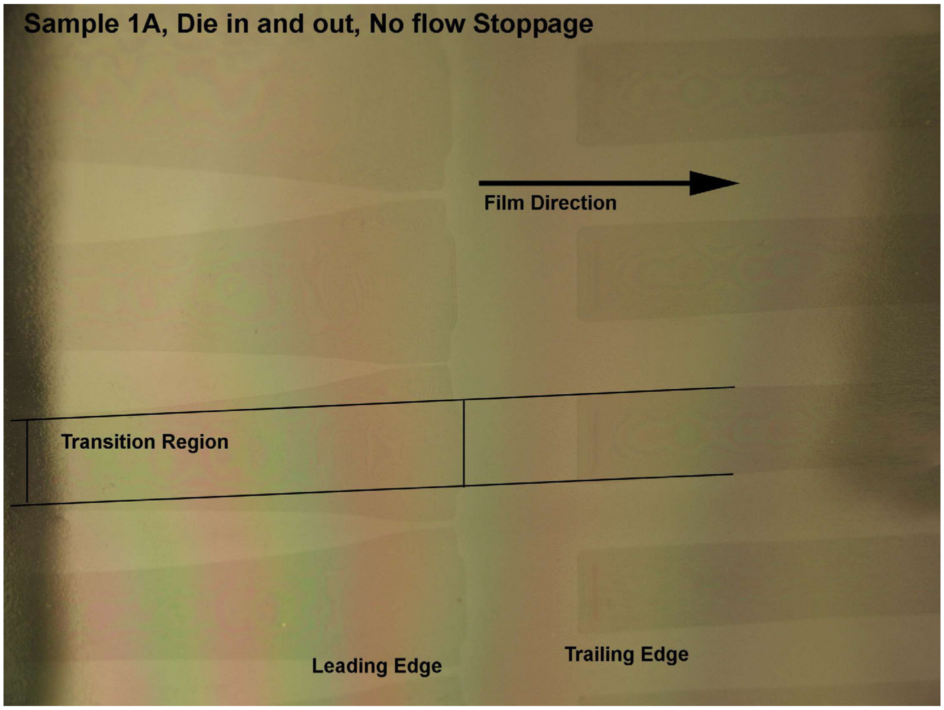


Figure 72. Stripe Coating, Sample 1A, die out and back with no flow stoppage

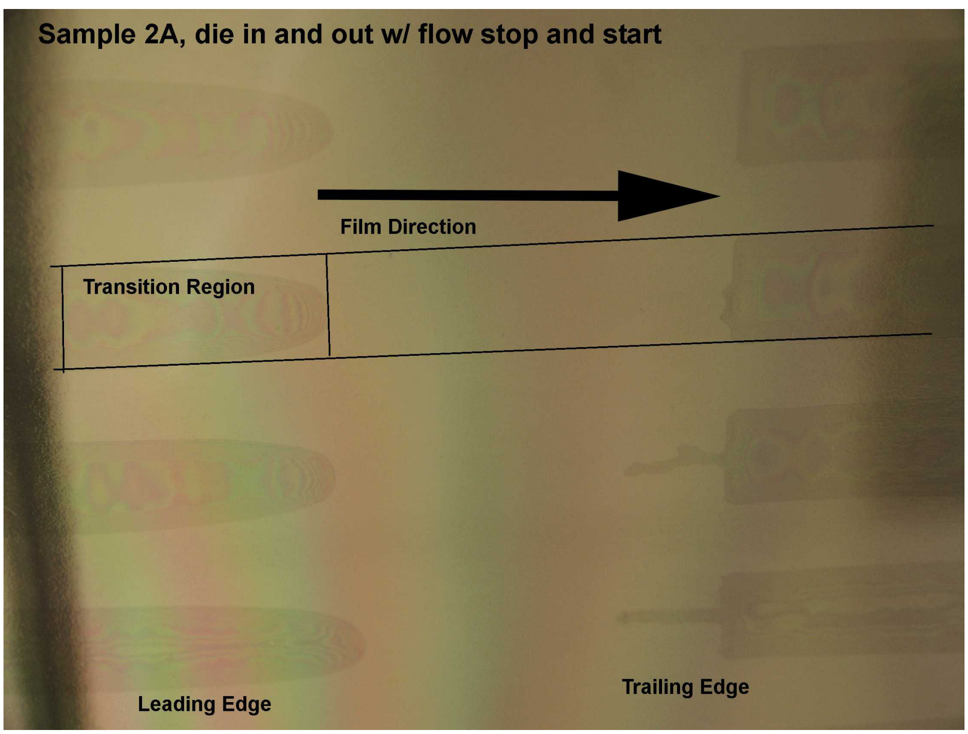


Figure 73. Stripe Coating, Sample 2A; flow stopped with die outage and started just prior to die coming back in. Shorter transition observed than seen in previous picture.

8.2.1.2 Discussion of Upgrades for Patch Coating Tests

To further pursue web patch coating, automation must be brought to bear to produce accurate results. The initial automation would include an automatic 3-way valve, and pancake air cylinders for short stroking the die head in and out quickly. A small PLC would be configured to accurately handle the precise timing of the automation. An optimum system would shut the flow off prior raising the die, and reestablishing the flow a short time before lower the die. It is believed with correct timing, we can refine the start of the fluid to minimize the length of the leading edge. This level of automation would produce better results than we experienced, but it does not address the vacuum transition effect. It would be best if we do not use a vacuum for short patches. The estimated cost for implementing the above automation is thought to be below $10,000.

Two higher levels of automation were discussed. Frontier makes precision piston pumps for their sheet patch coaters. A piston pump would allow the precise suck back of coating material into the die. It is not understood whether this idea is patented already by 3M, who has disclosed they use a small plunger on their patch coater. The second idea is stop the web until the coating bead is established between the die and film. This would involve installation of a dancer assembly, and an upgrade to the coating drive system to provide the acceleration rate required. Since this would now more closely resemble the technique used at FAS, it would not be worthwhile to pursue here at this juncture.

8.2.1.3 Stripe Coating Conclusions

This demonstration project proved the capability of Frontier, working under our direction, to stripe coat PLED devices. We believe that we can match the performance observed today with our LEP coating solution, but reducing all the edge non-uniformities would require some effort. With the automation described above and without the vacuum box, we should be capable of reducing the leading edge from 30 mm to 10 mm. Any further reduction would require one stop the web to establish the coating bead. Lower operating speed should also reduce the leading edge proportionally.

Frontier provides a friendly environment to conduct coating trials with very little sales pressure. They have a small Dynacoat system for less than $200,000 that could serve as an excellent in-house coating development tool. The unit would have the same coating station of their larger units.

An estimate of a capital investment of $10-20,000 and a minimum of 10-15 days of coating time ($2500/day) would be necessary to pursue the web patch coating option. Stripe coating of PLED polymer and PEDOT can be pursued at this time if we think it is a viable alternative.

8.2.1.4 PEDOT/LEP Coating Experimental

The experimental plan included two steps for each of four coating fluids. The first step was to do some simple optimization of the coating window by adjusting speed and assist vacuum. The second step was to coat a significant quantity at a standard condition for

further processing. Three of the fluids were PEDOT or modified PEDOT, the fourth fluid was the LEP which was coated on top of each of the previously coated PEDOT layers.

Only a few samples were taken prior to the windup to avoid an excessive amount of splices. LEP samples were cut out before the windup and taped to 6x6 glass plates. The glass plates were placed in plastic carriers for shipment. PEDOT samples were cut out before wind up and shipped back stacked on each other. More samples were cut from the roll inside the clean room back at Alien.

SETUP:

Slot Die Setup: Single Slot Die with 15 mil [3.8 mm] lips was setup using a 2 mil [50.8 μm] internal plastic shim

Coating Width: 5”

Film: 70 Ω/□ ITO coated on 0.005” [127 μm]Melinex, from NeoVac

Solutions Used:

- Bayer Baytron Lot #K0009
- AGFA Orgacon
- Zonyl FS-100, surfactant for Baytron
- 1% green LEP in xylenes

Pump: Micropump with 0.92 ml/rev pump head

Filter: Balston AQ grade 0.9 μm (98% retention)

Tubing: Solvent resistant L/S 24 Tygon tubing

Flushing: System was flushed with distilled water prior to the delivery of the Baytron. Tubing was discarded and the die was separated and dried after the PEDOT coating. The pump was flushed with Acetone.

See Appendix I for dryer setup diagram.

An attempt was made to clean all the rolls in the system that contacted the film, however it was noticed early in the second pass that a few rolls were missed prior to the slot coating head.

Web Speed: Due to the limitations of the pumping system, web speed was kept at 20 fpm [6.1 m/min] for the majority of the test.

Drying: PEDOT solutions were dried at 80 C in a 20 foot [6.1 m] dryer zone
LEP trials 15 through 20 used 130°C and 21 through 30 used 93°C temperature in the dryer. Residence time equaled 1 minute at 20 fpm [6.1m/min]. Air in the dryer passes through HEPA filters.

Room Cleanliness: The coating room was not a semiconductor grade clean room. It was closed off from the other areas with a set of doors, but did show some dust on the hard floor and on the flat work spaces. We wore Class 10,000 smocks and latex gloves. The film only saw the room conditions for about a minute as it was being unwound and rewound. Cut out samples spent a significant more time in the room conditions.

See Appendix I for a listing of the coating trials.

8.2.1.5 PEDOT/LEP Results

Coating Quality:
Coating conditions at Frontier were very different from FAS. The coating angle 20 degrees up versus straight down at FAS. Due to the pump limitations, the web speed was maintained at 20 fpm [6.1 m/min] for the majority of the test, roughly six times the speed at FAS. The coating lips were three times wider, and vacuum assist was required to maintain the coating bead at all the tested conditions.

PEDOT Coating:
Four PEDOT solutions were coated onto the bare ITO surface. The ITO surface was not cleaned or treated for enhanced surface energy. A mottled appearance was visible on the pure Baytron coating that was different from what was seen at FAS on bare clean ITO coated glass (Figure 74). The addition of isopropanol (IPA) did not improve the mottle appearance. The addition of Zonyl FS-100 did improve the appearance (Figure 75). Both the IPA and Zonyl additions reduced the ability of the solution to maintain the coating bead between the die lips and the film, thus reducing the coating operating window.

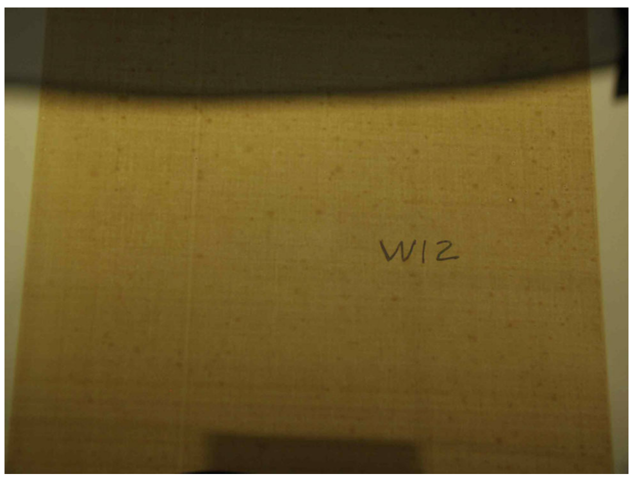


Figure 74. Condition #8, Pure Baytron coated on PET/ITO

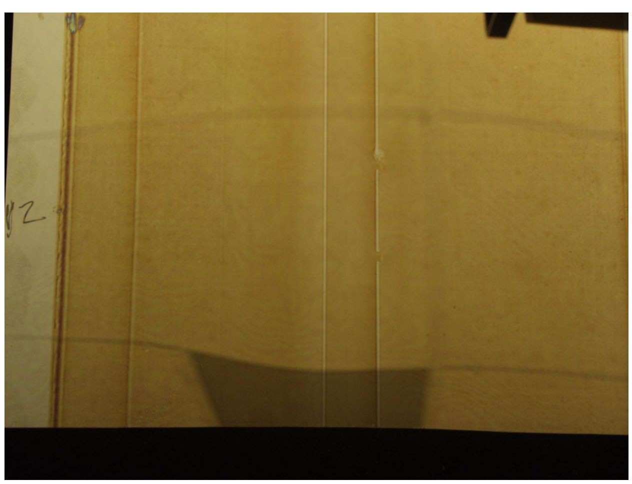


Figure 75. Condition #12, Baytron w/10%IPA and Zonyl coated on PET/ITO

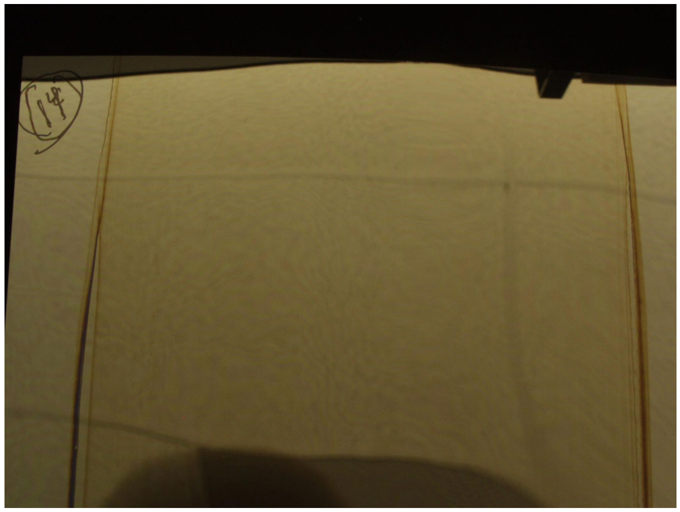


Figure 76. Condition #14, Orgacon coated on PET/ITO

As can be seen in the Figures 74 to 76, Orgacon provided the highest quality coating at these high-speed conditions. It also had a very small coating window, requiring a very tight coating gap and precise vacuum control.

8.2.1.6 LEP Coating

The LEP appearance was also not as uniform as the FAS coatings. The best coating was attained on the top of the Baytron/IPA(no Zonyl) surface (see Figure 78). The coating on pure Baytron had a 2" stripe going down the center that we could not eliminate during the brief trial (see Figure 77). The coating on the Orgacon had an uneven mottle appearance (see Figure 79).

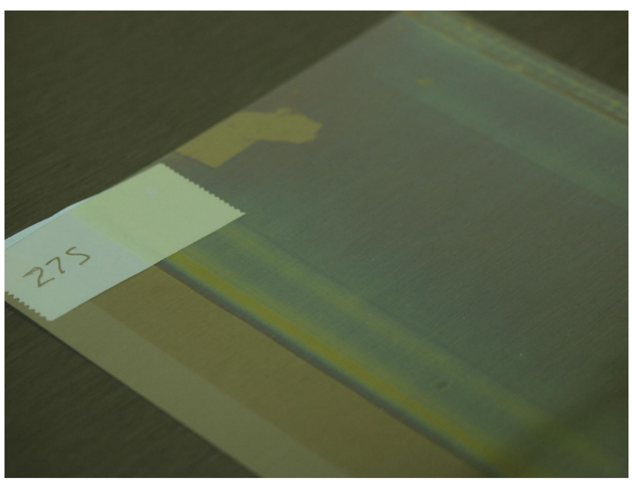


Figure 77. Condition #27 LEP on top of pure Baytron (converted in working device)

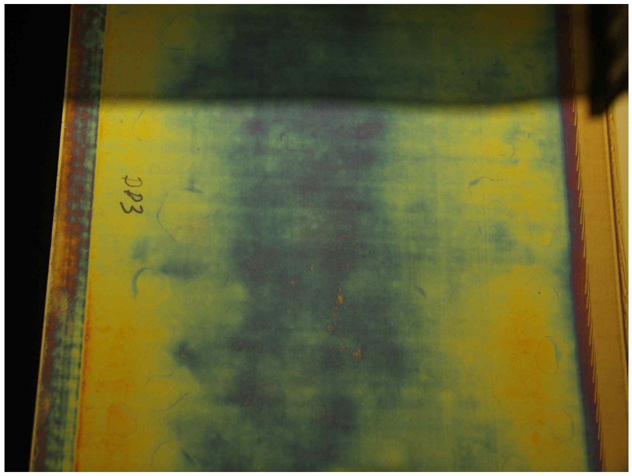


Figure 78. Condition #21, LEP on top of Baytron/IPA combination (sample unwound from roll – notice pressure rings along the edges)

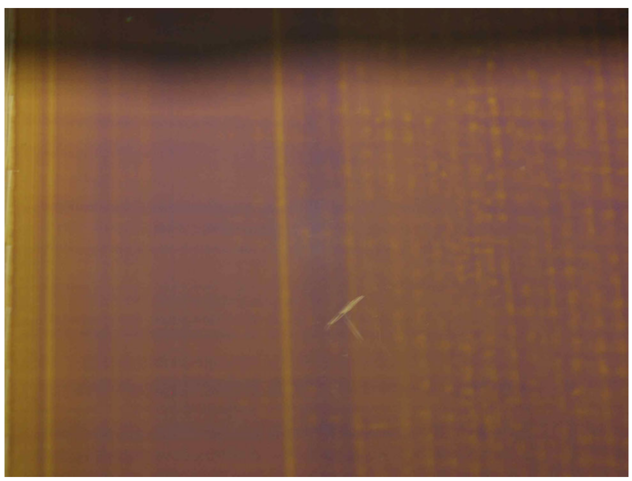


Figure 79. Condition #15, LEP on top of Orgacon

8.2.1.7 TV-1 Devices

Five sheets of film were made into TV-1 devices. Four of the sheets were sampled prior to the windup at Frontier with the LEP coating only touching one rubber covered idler roll. The samples were placed on glass and transported back to Alien in 6” [152.4 mm] square glass carriers. The glass supported the samples so the LEP coating would not touch any surface. At Alien, the samples were placed in a vacuum chamber until processing could be carried out. All the samples produced working TV-1 devices. Figures 80 to 82 show pictures of the working devices made from the coated Frontier film. Only one pixel devices measuring 10mm x 10mm were used for evaluation. The devices all had many apparent defects as can be seen in the photos below. One sheet was cut from the wound up roll of film that was transported from Pennsylvania to California. This sheet did not make a working device. We theorize that the winding causes too much damage of

the delicate LEP coating layer. Pressure spots could be seen on the LEP coating from being wound up (refer to Figure 78).

The I-V curve presented in Figure 83 is typical of all the working devices made. The rectification ratio was approximately 1 for the working device versus a typical value of 4000 for a device made on glass in a clean room. The device curves lie between the typical device and a linear resistance curve. There is no indication of the normal diode effect. The two most probable causes of the measured current leakage are contamination and damage of the coatings. The PEDOT travels over numerous rolls and is would up and unwound. The LEP does run over one roll prior to sampling. The luminance of this particular sample was also low, with the average value being 135 cd/m^2 at 10 mA/cm^2.

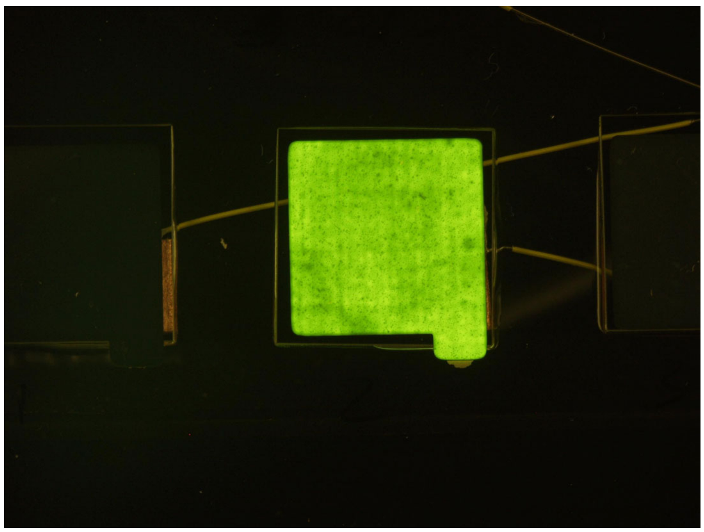


Figure 80. TV-1 Device from Condition #27, Baytron/LE

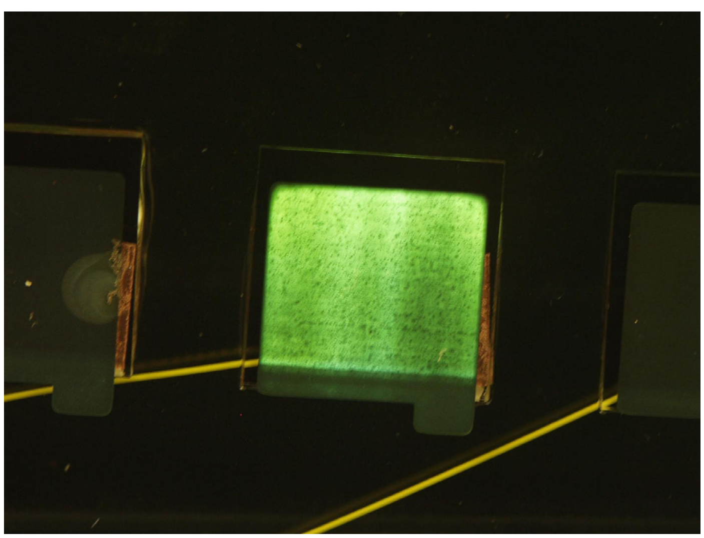


Figure 81. TV-1 Device from Condition #21, Baytron w/IPA /LEP

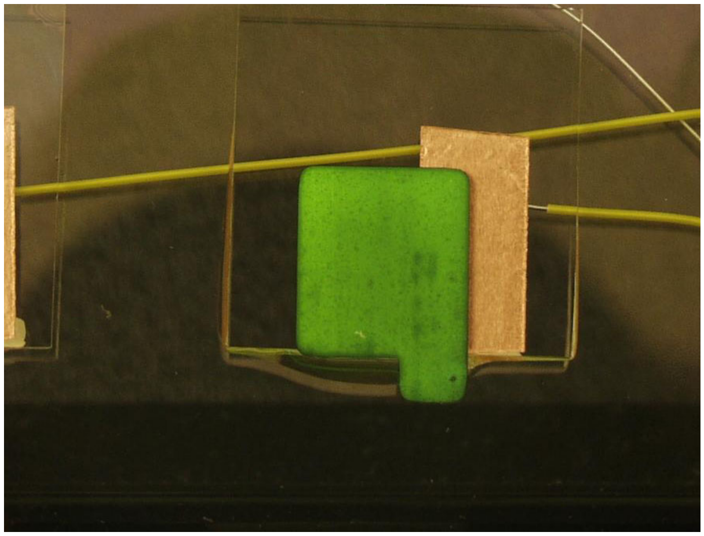


Figure 82. TV-1 Device from Condition #15, Orgacon/LEP

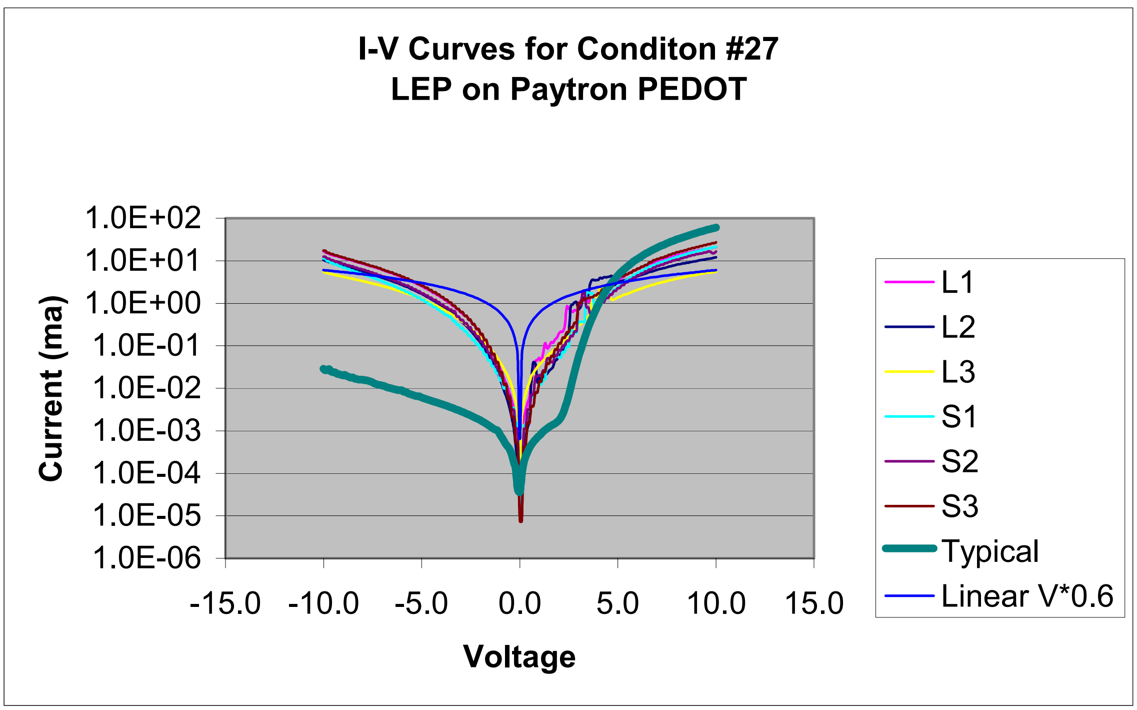


Figure 83. I-V Curve for Condition #27 TV-1 Device coated with pure Baytron.

Coating Window:

At 20 fpm [6.1 m/min] the coating speed was over eight times faster than the coating at FAS. Thus, the allowable gaps were much tighter and a vacuum box was needed to maintain the bead in the coating gap. For PEDOT coatings, the allowable coating gap reduced at the fluid surface tension went down. Baytron with a surface tension of 68 dynes/cm^2 was coated with a 100 micron gap. The gap stayed constant when the IPA was added, but

fell to 75 μm with the Zonyl addition. Orgacon with a surface tension of 25 $dynes/cm^2$ required a gap of 56 μm for a quality coating

8.2.1.8 PEDOT/LEP Conclusions

Overall, we gathered a large quantity of information in a one day coating trial. We had no significant mechanical problems with the coating system. It was encouraging to verify that we can coat at this high speed (20 fpm) [6.1m/min] in a potential production process.

Based on previous coating experience with coating PEDOT solutions, a large portion of the mottled appearance is coming from the condition of the film surface. With proper cleaning and treatment, a much better coating of pure Baytron can be anticipated. If that is not enough, we have established some background information for the use of surfactants in the PEDOT solution to improve the appearance. All the PEDOT coatings appeared hard enough to withstand the winding process without negative effects.

The LEP did not coat well on over material where a significant amount of surfactant was used. The result is different than demonstrated at FAS, and the first suspect is the increased speed. Mechanical contact with LEP surface after coating appears to be very detrimental based on initial results. We were not able to get working devices from film that was wound up inside the roll.

8.2.1.9 PEDOT/LEP Path Forward

Based on the encouraging results, the path forward should include additional coating trials at Frontier. The following issues should be addressed in a singular manner:

- With the use of better pumping system, go to lower speeds until machine chatter becomes an issue. Take one day prior to the run to thoroughly clean all rolls or cover rolls with a clean substrate. Wipe down floor and workspaces. Consider attaching additional filters on any H&V exhaust vents within the room.
- Have ITO film cleaned prior to the coating run. Consider using interleaf carrier to prevent the contact with film surface subsequent to coating.
- With cleaned and uncleaned ITO film, treat film for improved surface energy (corona discharge) prior to coating

8.3 Offset Gravure Coating

8.3.1 Introduction

The purpose of the offset gravure coating trial was two fold. Qualify the equipment and coater for potential future trials and to conduct some initial trial work on coating parameters. Roll coating offers the ability to impart shear into the material prior to and during the application of the coating material to the substrate. The amount of the shear imparted is higher than can be produced with the slot die coating method. The shear stress can be

adjusted with roller speed ratios or by the number of rolls in the coating train. The shear rate is also a function of the rubber roll hardness and the solution viscosity. It is possible that this shearing action will be necessary to align the polymer molecules for improved functionality of the light-emitting polymer. As a reference, it is known that shearing action of roll coating has improved the performance of liquid crystal polymers coated for polarizing purposes.

In offset coating, the coat weight is mainly controlled by the cell size of the gravure roll, which applies the coating fluid to the engraved rubber roll. However, this can be adjusted up and down by the speed ratio of the rolls and the rotational direction. When the rolls are going in reverse direction, roughly 35% of the cell volume is transferred to the engraved roll. About 65% is transferred when both rolls are going in the same direction. Reverse transfer is typically used in coating operations to reduce the chance of introducing ribbing defects.

8.3.2 MEGTEC Overview

The principal business of MEGTEC (Green Bay, WI) is supplying high efficiency dryers and emission abatement equipment to the printing and converting industry. The company ranks in the top 3 worldwide in terms of technology and size. The pilot line is maintained for research purposes and to assist with qualifying MEGTEC's dryers for new applications.

8.3.2.1 MEGTEC Experimental

- Dryer Setup: 66°C, 200, 450 and 750 Pa, Flotation Air Nozzle Pressure for Zones 1, 2, and 3.
- Dryer tension set at 3 pli [53.6 g per linear mm] Solution 1: 1.2% aqueous PVA solution, 0.12% Zonyl FS, color provided by Aldrich Brilliant Blue, 20,140-5 and Aldrich Brilliant Crocein M00, 21,075-7.
- Solution 2: Bayer BaytronP
- Solution 3: 1% PVK dissolved in dichlorobenzene.

- Printco Enclosed doctor box with stainless steel blades
- Gravure Roll #3, 110 Quad, Ref. #67, 26.9 BCM cell volume
- BunaN engraved roll was produced at Flexcraft.
- Roll gaps set at minimum impression to achieve good transfer.

- The gravure and engraved rolls were each controlled by separate drives. One improvement needed for future trials is the need for the engraved roll drive to remain running and nipped to the gravure roll when the line is stopped.

8.3.2.2 MEGTEC Result Summary

Four patterns were looked at on the samples: 1) dot pattern template, 2) continuous 2" [50.8 mm] wide stripe, 3) large 2"x2" [50.8 mm x 50.8mm] square patches, and 4) percent fill engraved screen pattern template. The PVA and Baytron gave similar results unless noted otherwise. The PVK results are not reported due to severe repellency of the solution from the polyester in the drying process.

The dot pattern contained circular dots with the following diameters: 1000 µm, 500 µm, 300 µm, 200 µm. and 100 µm. Dot pattern was typically printable down to the 200 um dot, with one Baytron sample recognizable down to 100 µm. However, the idea of forming a small dot of coating with a flat plateau and sharp sides does not show much promise based on the initial results. Drying and surface tension effects produced craters of coating on the surface. Figures 85 and 86 show WYKO surface height maps (profiles) of two dots printed with the PVP solution. Similarly, Figures 87 through 90 show the surface profiles of PEDOT printed dots as they decrease in size from 1000 µm to 100 µm in diameter. The PEDOT did produce more of a plateau inside the crater than the PVA.

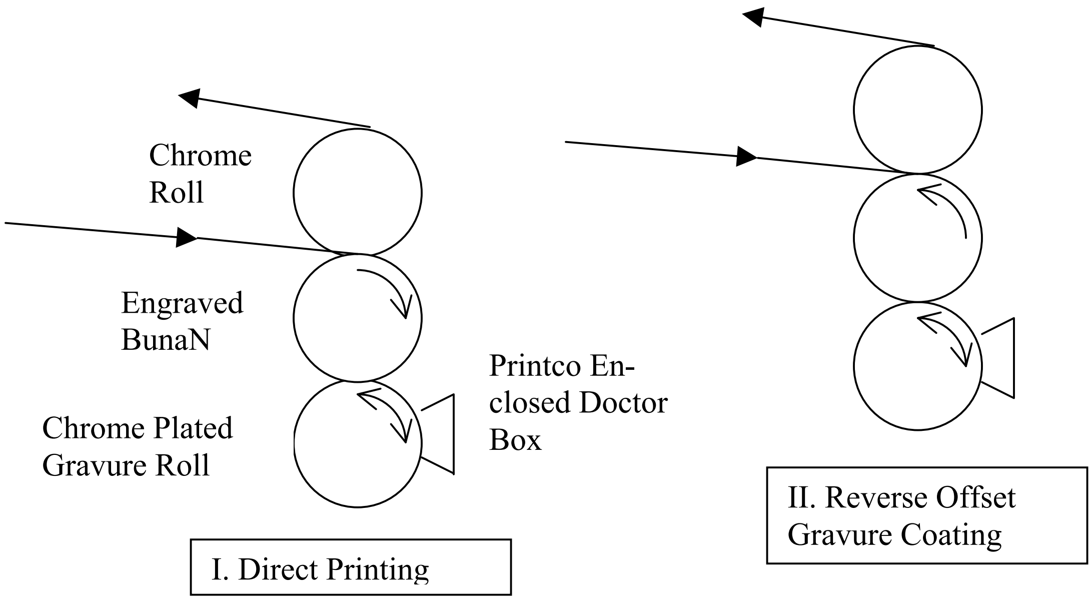


Figure 84   Megtec coating head configuration

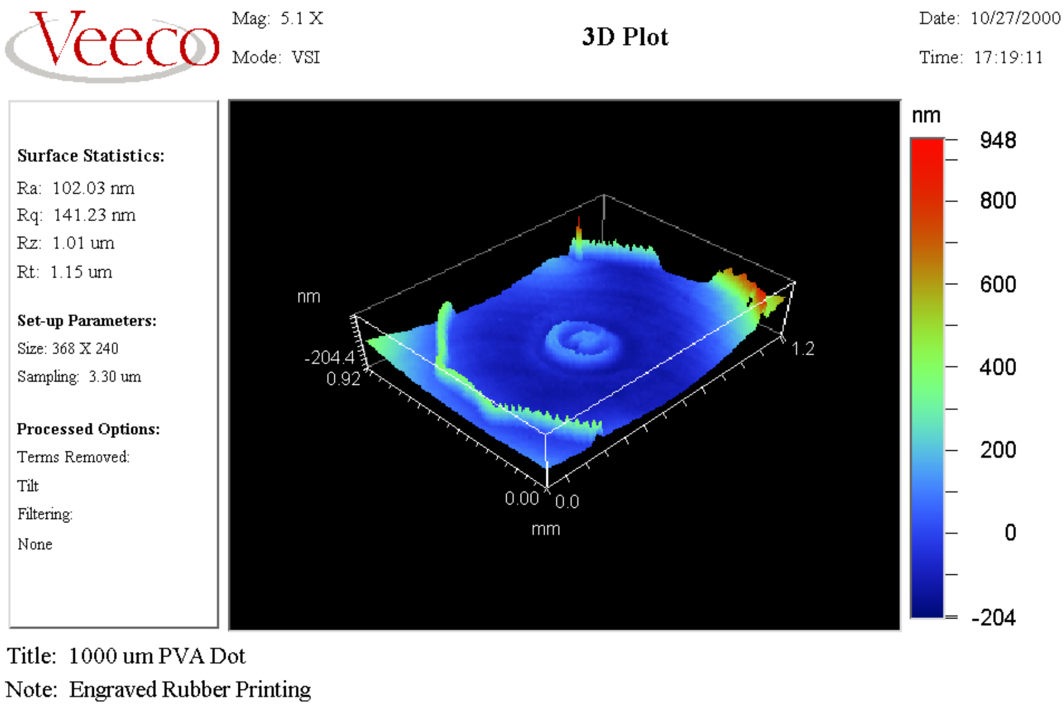


Figure 85. Surface topography by WYKO of 1000um PVA dot; crater formed during the drying process.

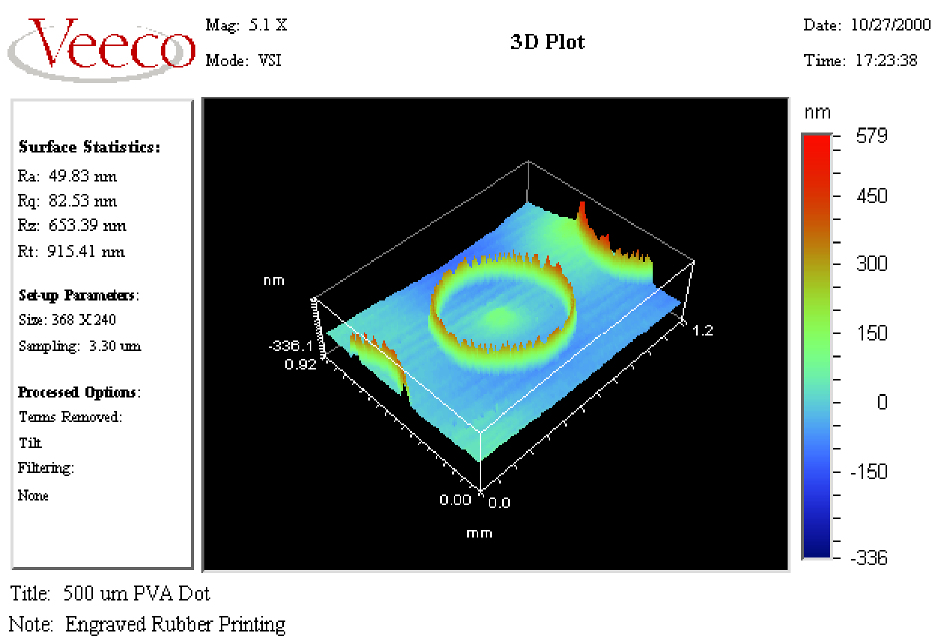


Figure 86. Surface topography by WYKO of 500um PVA dot; crater formed during the drying process.

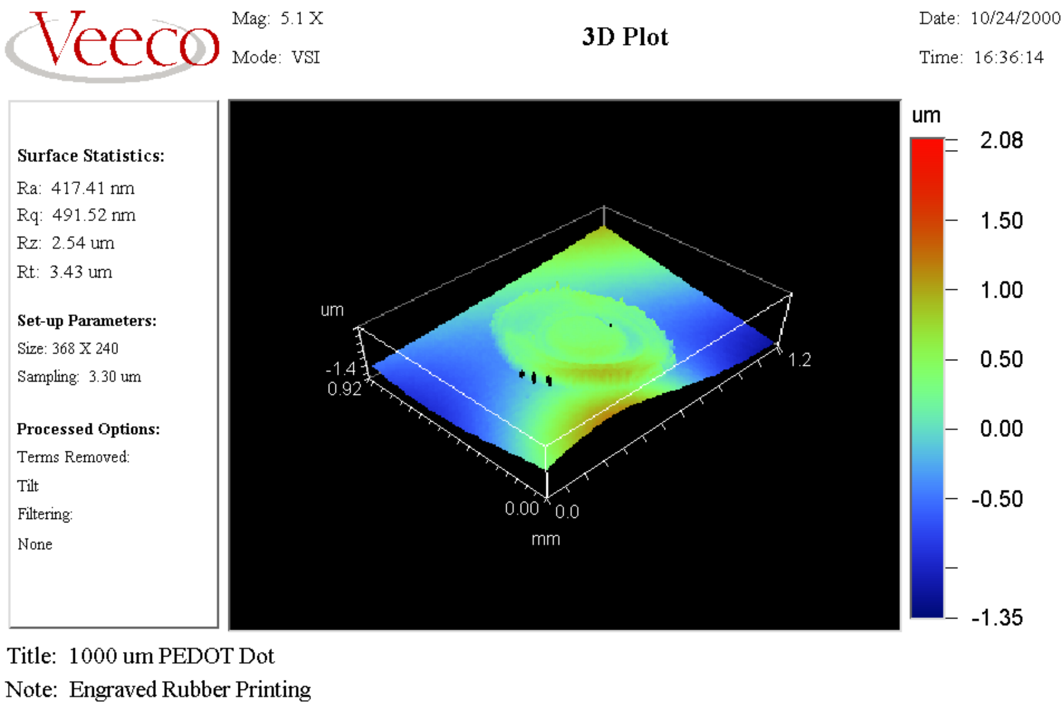


Figure 87. Surface topography by WYKO of 1000um PEDOT dot; improved surface topography.

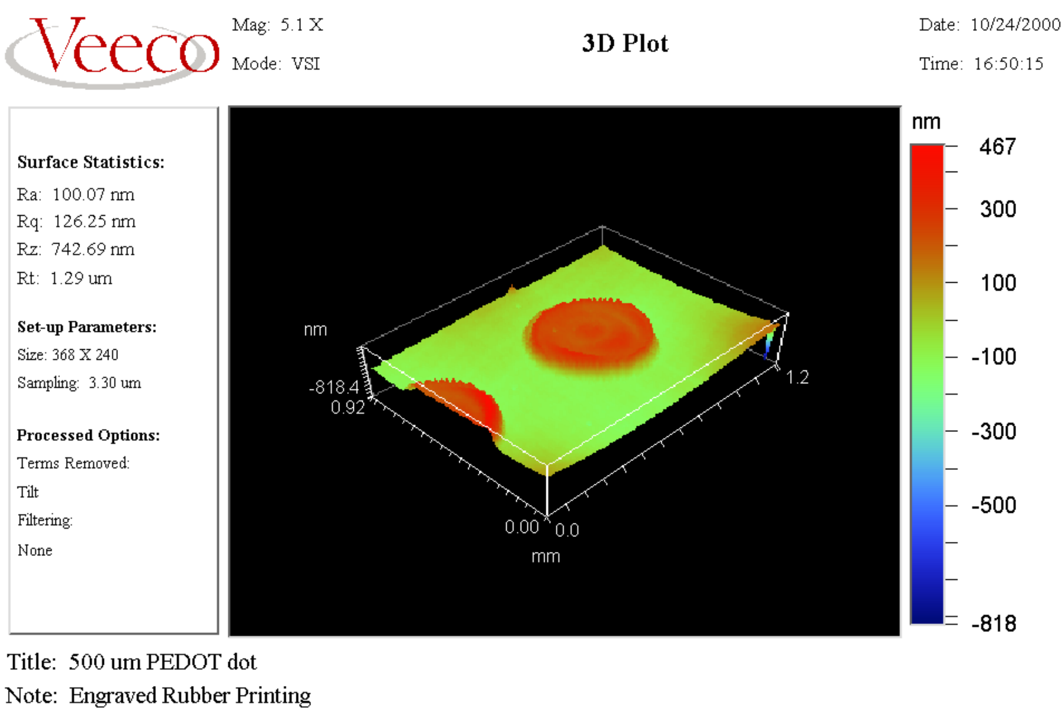


Figure 88. Surface topography by WYKO of 500 um PEDOT dot.

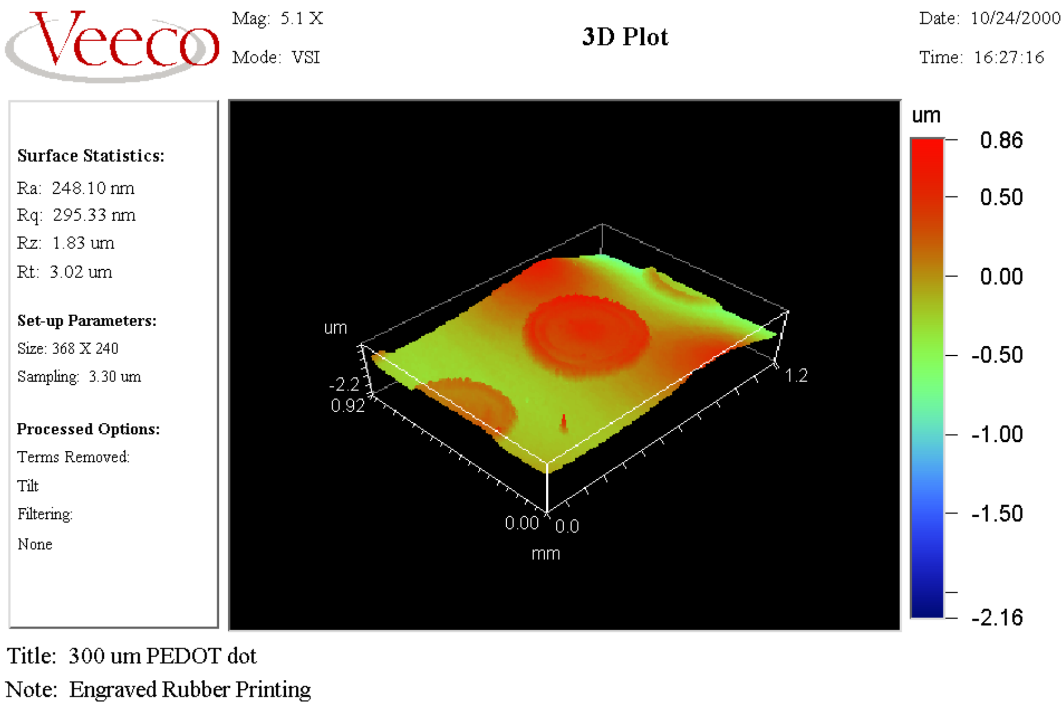


Figure 89. Surface topography by WYKO of 300 um PEDOT dot.

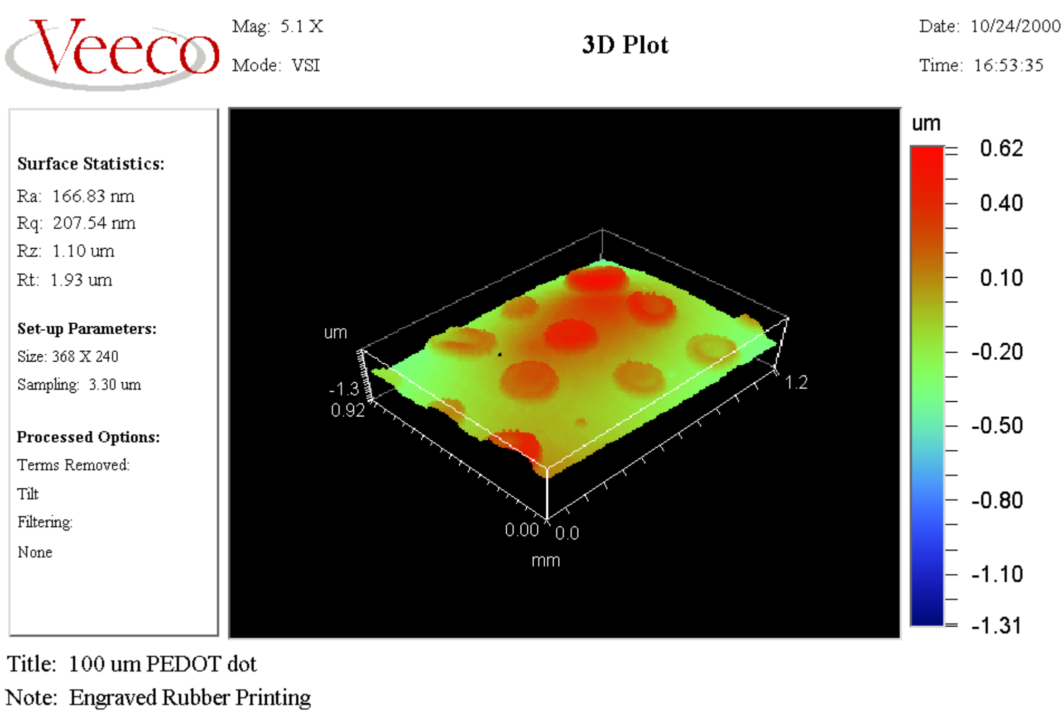


Figure 90. Surface topography by WYKO of 100 um PEDOT dot with diminished crater formation.

The continuous coating using the offset gravure technique produced very uniform coatings with all three solutions. The edges were also very sharp, with 500 um or less of non-uniform area. A method for measuring the coat weight has not been established yet. The substrate is not flat enough to get meaningful thickness data from the Tencor or the WYKO instruments.

The square patches did not produce a uniform patch of coating. In the reverse mode, the patch would start thin, build up to a uniform coating, and then release a large amount of coating at the end of the patch. The release amount being a buildup of coating in the impression nip (see Figure 91). This build up is a function of the roll speed ratio and viscosity. A higher viscosity material would lead to a lower buildup. In the forward mode, no coating was transferred until the end of the patch at which time a puddle of fluid was allowed to go through the forward nip onto the web.

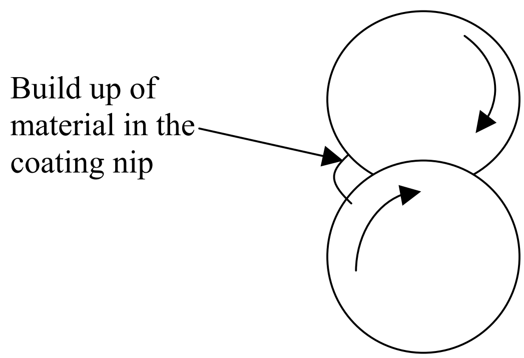


Figure 91. Diagram of material build up in reverse transfer mode.

The percent fill screen test pattern produced samples in the direct printing and the reverse coating modes. The pattern consisted of attached blocks, which went from a 5% fill to 100% fill. In reverse coating, the pattern gave a gradual building of coat weight as the % fill increased. Thus, this is an additional means to vary the coat weight. The Baytron material did not produce a continuous film until the 80% fill was achieved. Between 5 and 75% fill, the film was not thick enough to overcome the surface tension forces of the fluid pushing it to break up.

Compared to the stripe coating, there was more non-uniformity present in the bulk of the coating and the edges were not as crisp. With direct printing, the PVA formed a continuous film at 35% and Baytron at 85% fill. Between 35 and 65%, the PVA film had an orange peel pattern which went away at 70% fill.. The end of the patch still had the heavy trailing edge seen on the non-engraved patches. In a typical printing operation, a 90-95% fill is usually used to produce the solid colored areas. It is our belief that the low viscosity of our fluid was the principal culprit for the heavy trailing edge of the patch. A dam of fluid is being built up in the nip, because the hydrodynamic forces are unable to overcome the mechanical forces.

The BunaN roll held up well to the dichlorobenzene. No visible softness or pattern deformation was observed in the brief time that it was present on the roll.

8.3.2.3 MEGTEC Conclusions

In respect to fluids, the surface tension of the Orgacon allows it to cover a variety of surface imperfections, while the Baytron will tend to show every one. Even in the best stripe coating samples of Baytron, small repellencies are present. There appeared to be some kind of incompatibility between the PET and the PVK coating solution, which is not understood at this time. Viscosity and % solids are coating solution parameters, which will need further study.

The stripe coating technique worked well with the Baytron and PVA aqueous solutions. Our current inability to measure the coat weight is only a small detriment in analyzing the result, but one that we need to be rectified in the future.

The equipment will be sufficient for crude testing only. The major shortcomings are that it is not located in a clean room, considerable chatter is present at the minimum line speed of 10 fpm [3.05 m/min], and the coating back up roll is not driven.

One improvement has been suggested for future trials. Currently the engraved rubber roll disengages from the gravure roll and stops when the film movement is stopped. This allows the coating material to dry up on the rubber roll. With some simple rewiring, it should be possible to leave the engraved rubber roll engaged with the gravure roll while the film line is stopped.

8.3.2.4 MEGTEC Path Forward

Once methods have been established to analytically determine the morphology of the polymer and its effect on luminescence efficiency, an additional trial at MEGTEC would be in order to gather sample of polymer coated with this technique.

In terms of coating dots, a literature study is needed to better understand the effects that viscosity and drying conditions play in creating the craters. If a reasonable viscosity and/or drying process have a chance of overpowering the surface tension forces to produce a flat plateau dot, an additional trial would be warranted.

For patch coating, another possibility to achieve the patch would be direct gravure coating vs. the offset technique. This technique does not provide a means to adjust the shear rate.

8.4 Web Coating Summary

The web process development resulted in better understanding of the challenges ahead of us in our future efforts to transfer the manufacture of PLED on integrated NB backplane from sheet to web substrate. Despite the limited trial runs at vendors, we were successful in producing working devices using slot die coating, opening another opportunity for

economical coating of web substrates with PLED materials which saves about 95% of waste experienced with standard spin coating.

However, our attempts to expand into the area of coating (printing) patterns, whether it was a patch coating by slot die, or dot coating by offset gravure, ran into great difficulties. There is strong interaction between surface preparation, transfer of the solution material and drying, all of which must be very well controlled.

To develop the continuous slot die coating of PLED materials to its full potential, an in-house laboratory coater is necessary. We believe that the coating of PLED materials by slot die coater for production of monochrome displays and other emissive devices would be a technological breakthrough similar to the impact of inkjet printing of polymers on fabrication of color PLED displays.

9. BARRIER LAYER TESTING

As indicated earlier, a hermetic packaging is a necessary prerequisite for fabricating PLED devices with practical life span. Essential parts of such hermetic packaging are barrier layers either deposited on the plastic film at vendor, or incorporated within the PLED device at Alien. In order to evaluate the flexible PLED barrier layers provided by various vendors, we started a coarse screening test known a as "lid test." Regular PLED devices fabricated on ITO/glass were encapsulated with these barrier materials (the glass lid was substituted with a lid consisting of a plastic substrate with barrier layer(s) on its surface(s)), and stressed under constant current of 10mA/cm^2. Devices encapsulated with glass on the same substrate were used as control samples for the stress test. The tested devices were placed in the Test Rack (Chapter 3.0), which was located in our warehouse.

The reader is reminded that the black spots shown in glass encapsulated devices are result of our non-optimized PLED processes, as discussed in the Chapter 2.0, and should be ignored when evaluating the barrier layers (black spots always occurred on our samples providing enough time for them to develop). Only black spots in excess of the density and size observed on control glass encapsulated samples were used for evaluation of the barriers.

9.1 Vitex Barrier Layer

The Vitex barrier layer (Vitex Systems, Sunnyvale CA), with the trademark Barix, is based on alternating of organic and inorganic thin films, deposited in a proprietary process. The organic films provide fresh surface for the following inorganic film, thus disrupting the growth of defects through the stack. We tested about six different Vitex samples of barrier layers deposited on one side of the PET film.

Our preliminary tests suggest that 19E and 23E have the best performance. Devices encapsulated with barrier material 23E (Figures 96 and 97) and 19E (Figures 98 and 99) showed only slightly larger black spots than the control devices after being stressed for 24 weeks. Devices encapsulated with all other barrier samples showed marked defects in excess of the control samples after being stressed for 2-8 weeks. These results suggest that the size and number of pinholes in the two barrier layers (19E and 23E) are small enough to make the barrier almost impervious to oxygen and/or water. Some of the Vitex barriers showed quite promising performance, though further improvements are required in order to fully satisfy the requirements for PLED application. According to Vitex, other OLED/PLED manufacturers also tested their layers directly on OLED/PLED displays with a proven practical lifetime of three to six months.

9.2 Dow Barrier Layer

The barrier layers from Dow Chemical (Midland MI), Dow #1 and Dow #2, were also evaluated using the lid test. Their barrier layer is based on proprietary process employing

chemical vapor deposition of SiO2 on both surfaces of the plastic substrate. Unfortunately, the performances of these barrier layers were much poorer than of the Barix barriers. Devices encapsulated with Dow #1 and #2 samples stopped emitting light (overlapping large black spots) within 1 to 2 weeks of the stress test.

Figure 92. Fresh PLED devices encapsulated with Vitex 23B barrier (left) and with cover glass (right)

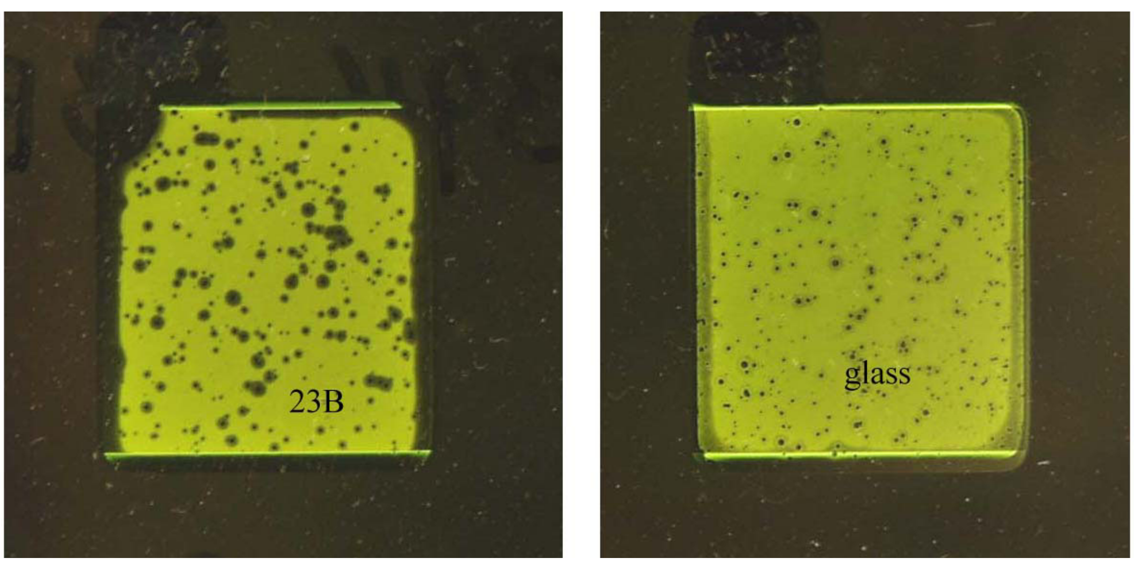


Figure 93. PLED devices encapsulated with Vitex 13916-23B barrier (picture on the left) and with a piece of cover glass (picture on the right) after stressed for 24 weeks at 10mA/cm2 in warehouse environment.

Figure 94. Fresh PLED devices encapsulated with Vitex 19E barrier (left) and with cover glass (right)..

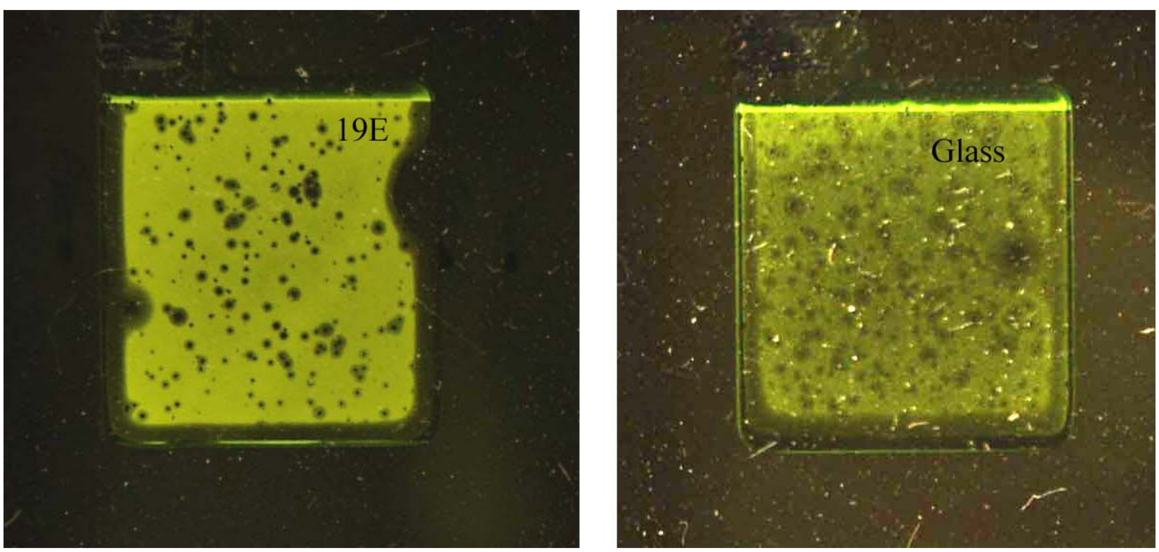


Figure 95. PLED devices encapsulated with Vitex 13916-19E barrier (picture on the left) and with a piece of cover glass (picture on the right) after stressed for 28 weeks at 10mA/cm2 in a warehouse environment.

9.3 Summary

The Barix barrier materials showed promising performance in a number of tests using our materials system. While the lifetime of PLED devices was encouraging, the Barix barriers did provide a significant challenge in integration into the Alien NanoBlock IC process. Specifically, in many PLED device constructions it is necessary to place the Vitex barrier on top of the substrate containing the NanoBlock ICs. In order to make electrical contact to the NanoBlock IC drivers, it is then essential to be able to reliably etch via holes and make metallic interconnects to the NanoBlock ICs.

This via formation process proved very difficult with the Barix barrier materials. The Vitex stack was quite resistant to dry etching, and Alien was never able to develop a suitable patterning process. While it is certainly possible that such a process could be developed, this difficulty in etching led Alien to consider alternative barrier materials that could provide both good protection and allow for dry patterning. This work is described in the next section.

10. DEVELOPMENT OF A MULTI-STACK SIO2/SOG FILM AS A HERMETIC BARRIER FOR PLED DEVICES

10.1 Introduction

As noted in Section 10, a robust barrier against water and oxygen permeation is an important component of PLED devices. For the flexible displays under development by Alien, an additional need is the ability to pattern this flexible barrier to allow electrical connection between the embedded NanoBlock ICs and the display pixels. An illustrative example is given in Figure 96.

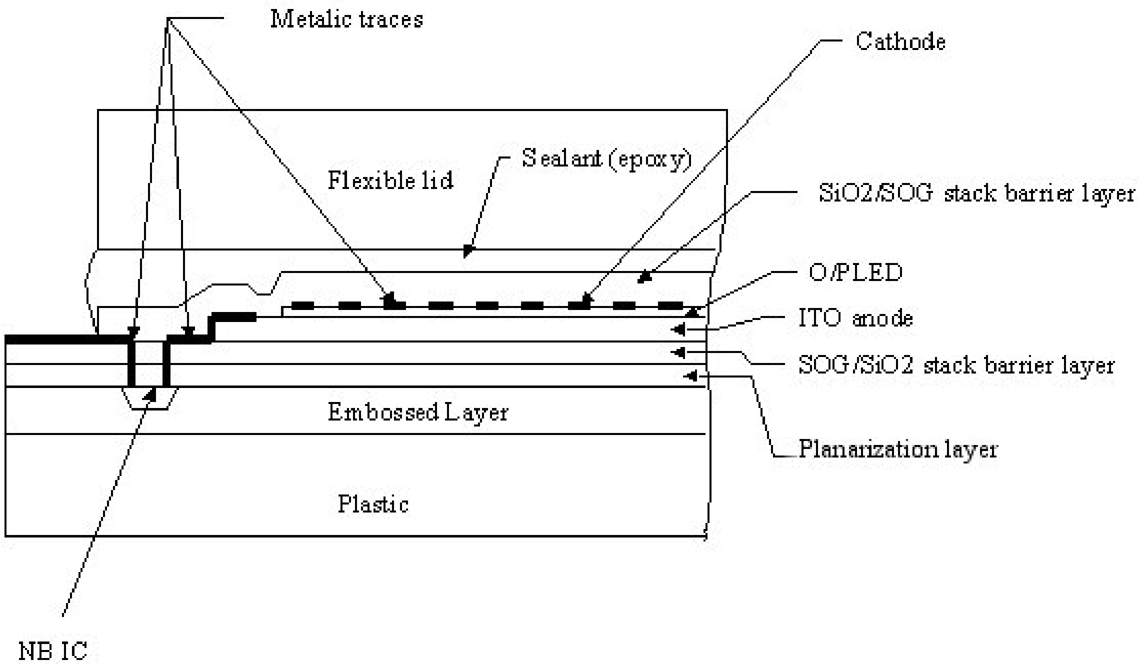


Figure 96. Schematic of an Alien PLED device on plastic using NanoBlock IC (NBIC) drivers.

Developing such a barrier is challenging. First, many transparent barrier materials tend to form pinholes during deposition. The transparent barrier material has to be resistant to the formation of pinholes throughout the entire barrier. Secondly, many transparent barrier materials contain a substantial content of organic materials to lend it flexibility. These organic materials suffer from instability or even bubbling when exposed to heat, ultraviolet or visible light, or oxidative agent such as ozone. It is desirable that the barrier material has no content of organic materials, or to use organic materials that are insensitive to these conditions. Finally, there has to be an easy means to etch through the transparent barrier to form electric contacts between layers.

A promising transparent barrier film for PLED devices is “Barix” film, which consists of a multi-stack of polymer/Al_2O_3 layers. Several problems are associated with this type of barrier, however. It is extremely difficult to etch through. Additionally, in our hands we sometimes found some instabilities in film quality upon exposure to baking and

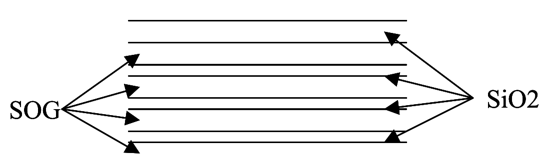
UV/Ozone cleaning during subsequent processing. These difficulties made integration into Alien's development display devices problematic.

10.2 Alien Barrier Film

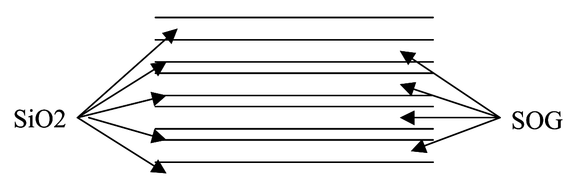
Based on the above requirements, we proposed to use a multi-stack of a spin-on glass (SOG) and vacuum-deposited silicon dioxide (SiO_2). We have found that such multilayers appear promising as a hermetic barrier for PLED on plastic. SOG can be spun on with a typical thickness of 500A to 5 micrometers, and SiO_2applied by sputtering or other means, with a typical thickness of less than 1 micrometer. Both SOG and SiO_2 are quite transparent in visible light.

A perfect SiO_2 film itself, in principle, can be an effective hermetic barrier layer. Unfortunate it is inevitable to have such defects as pinholes in SiO_2 films regardless of deposition method, through which water and oxygen and can readily penetrate. Spinning on SOG can effectively block these pinholes. A multi-stack of such double layers should result in an effective hermetic barrier. In most cases, the stack will start with SOG and end with SiO_2. There is no requirement that all the layers are the same thickness, and the top SiO_2 can be thicker than that in the intermediate layer. This concept can also be used as a top barrier. In these cases, where the top layer to be covered is sensitive to organic solvent or prone to oxidation (such as the cathode metal Ca and Al), the dry-processed SiO_2 would be the first layer. This stack can start with a thicker SiO_2 layer, 1200Å to 2000Å, for example, to protect the underneath material. A typical thickness for SOG and SiO_2 would be 1500Å and 800Å respectively, and the thicker top or bottom SiO_2 2000Å.

When the barrier is deposited directly on plastic, this double glass barrier can offer effective planarization. Often, a plastic substrate is defective in pitting and particles, causing pinholes in barrier and compromising PLED devices performance. A Thick SOG layer can be applied first to planarize the surface and cover the defects. Fig. 2 a) and b) show two typical such stacks.



a) A barrier stack starting with a thick SOG to planarize surface and cover defects on plastic.
Ideal for bottom P/OLED bottom barrier



b) Another barrier layer stack starting with SiO2 to protect sensitive underlying sensitive material.
Ideal for P/OLED top barrier

Although there are many types of SOG materials that are transparent after being cured, it is however preferred to choose the ones that have low shrinkage upon curing and are

highly crack resistant. One example of this type of SOG are those derived from the methylsiloxane family, although others certainly exist.

Typically, a SOG requires much higher curing temperature than what a plastic substrate can tolerate. We have found, however, promising results for films cured at much at150°C. We anticipate that, with longer baking time, or, at room temperature with IR lamp radiation, the film could be adequate for the application. The higher the curing temperature, the more condensed the film is.

Such a hermetic layer cam potentially be easy and economic to produce. SOG can be easily applied by many ways such as spinning, dipping, printing, slot coating, or exposure to mist. SiO_2 can be applied by sputtering, evaporation, or various CVD processes. Cured or partially cured SOG has excellent adhesion to SiO_2 surfaces and is known for its excellent gap filing capability. The combination of SOG/ SiO_2 is already used in semiconductor industry as an effective planarization layer. This stack can be readily dry etched by conventional fluorocarbon-containing plasmas and provide a controllable sidewall profile, which is crucial to make a good electrical contact through vias. It is also possible to wet etch with HF containing solution. Since the entire stack is largely made of inorganic material, the decomposition of organic material upon exposure of UV/Ozone or plasmais not expected, and should minimize the formation of bubbles and other instabilities in the barrier film.

10.3 Barrier Film Fabrication

The SOG layer in the stack is applied by spinning from a conventional Karl Suss photoresist spinner, and SiO_2 by vacuum sputter deposition. The SOG solution used in our experiments were either AccuGlass 111 or 312B, purchased directly from Honeywell. Both systems are methylsiloxane $[(CH_3O)_4\text{-Si}]$ based. The main difference between them is in solid content, resulting in different thickness of cured film.

Figure 98 shows the final film thickness change with spin speed for both formulations. Typically, 312B is used as the first layer to render a thicker layer to cover the defects on

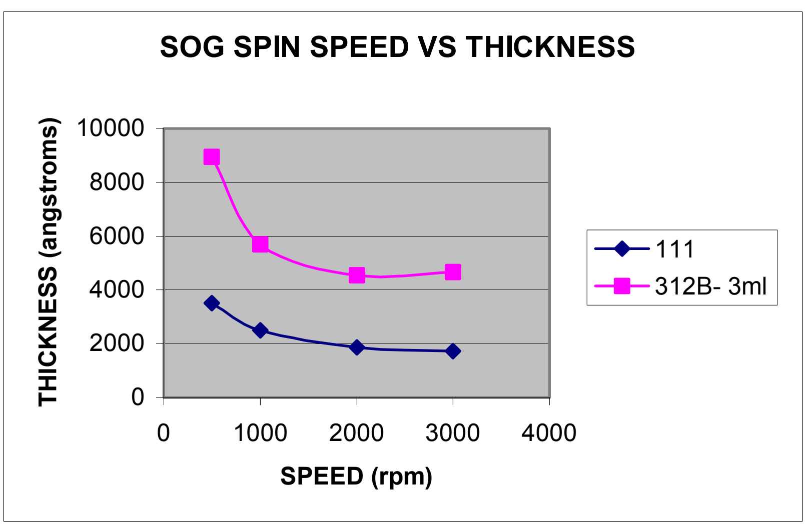


Figure 98.   Spin-on glass film thickness changes with spin speed

the plastic substrate. For the subsequent layers between SiO_2, the 111 material is used.

According to the manufacturer, fully curing the film requires a bake at 425°C. In this curing process, the SiO-R or SiO-H bonds in the precursor are broken so that Si and O form a crosslinked polymer. Figure 99 shows the corresponding microstructure. (R=CH3) In case of partial curing, some of the O will be terminated by H or even CH3, so the film will be less cross-linked and therefore less dense. A typical set of processing conditions for the barrier stack is listed in Table 6.

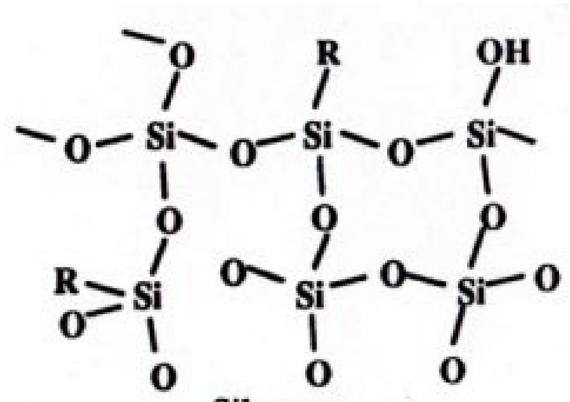


Figure 99. Representation of molecular structure of cured spin on glass

Table 6. Barrier stack processing conditions

Process	Recipe
Ultrasonic clean the plastic substrate in detergent for 10min and SRD	30:1 water to Versa-Clean from Fisher Scientific.
O_2 plasma surface treatment	Corona treatment, 4 passes@ 0.6kw, 3-4 ft/min
SOG 312B spin	312B 100rmp/5sec/100ramp/1000rmp/20sec/500rmp 1min bake at 80°C, 60min bake at 150°C
SiO_2 deposition	20 sec. Presputter clean, 900Å thickness
SOG 111 spin	100rmp/5sec/100ramp/3000rmp/20sec/500rmp 1min bake at 80°C, 60min bake at 150°C
SiO_2 deposition	20 sec. Presputter clean, 900Å thickness
SOG 111 spin	100rmp/5sec/100ramp/3000rmp/20sec/500rmp 1min bake at 80°C, 30min bake at 150°C
SiO_2 deposition	20 sec. Presputter clean, 1300Å thickness

10.4Results

A barrier film was built on a PET plastic sheet as described above. No bubbling of the barrier film was observed either during baking or exposure to UV ozone. To demonstrate compatibility with the PLED materials and processing, a PLED device subsequently formed on top of it. Figure 100 shows a photo image of the lit device and its I-V curve.

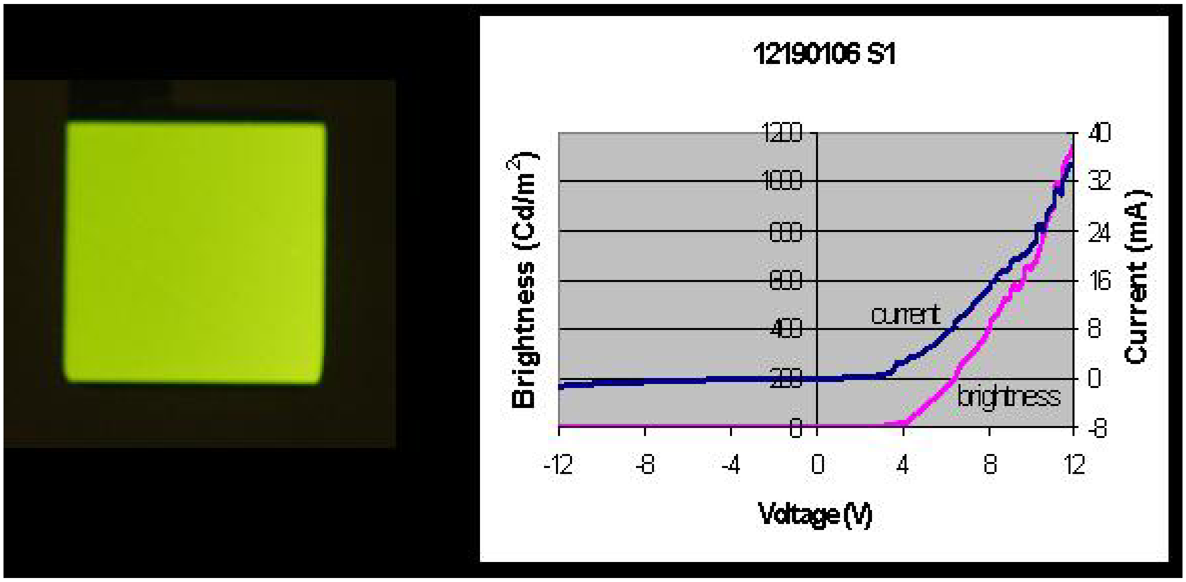


Figure 100.   A PLED built on Alien barrier layer

We have also demonstrated that the barrier layer can be dry etched using a conventional RIE system with CF4 as is shown in Figure 101. The feature size in the image is 40 μm. Using photo resist as mask, a gentle sloped sidewall can be easily achieved for forming a reliable electrical contact across the barrier film.

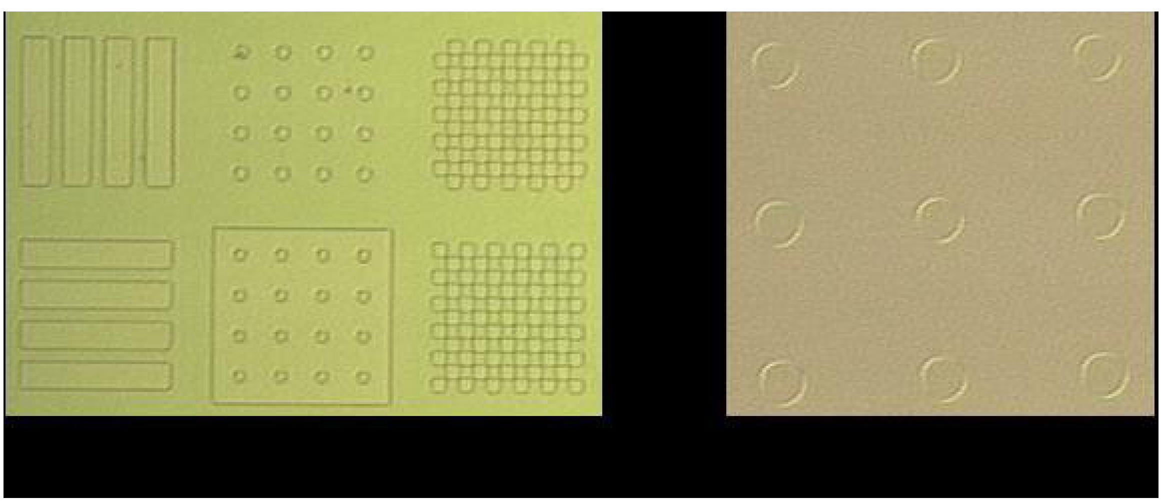


Figure 101.   Patterns demonstrating fidelity of dry etch process of Alien barrier film using a RIE system

To assess its effectiveness as a hermetic barrier, four 4” square sheets of the film were sent to Mocon Corp. to measure permeation rates of water and oxygen through it. The test report is shown in Appendix J. With 100% oxygen at 1 atm, the average permeation rate was 0.0024 cc/day/m^2. With 100% RH moisture vapor in nitrogen gas at 23 °C, the permeation rate below test limit of 0.005 g/day/m^2.

The oxygen permeation rate from this test is higher than what would be required of a hermetic barrier, but we still believe that these results are promising for a variety of reasons.

- Little process and materials optimization has been carried out to date, in which PLED film stability has been the primary criteria. We believe that a structured development program would likely lead to improved barrier properties.
- The MOCON results can be heavily weighted by the presence of pinholes. Functional PLED lid tests can provide better information on whether the permeation observed is constant through the film or dominated by pinholes.

10.4.1 Life and Reliability Test

Two types of devices were made to perform the life and reliability tests on the barrier film. One is cathode metal test, in which cathode metal (Ca or Ca + Al) was directly deposited on a clean soda lime glass and sealed with the barrier film using UV curable epoxy. In a second test, functional PLED devices were built on soda lime glass and sealed with barrier film using epoxy. In both cases, the barrier film was first diced with laser beam into small 1.5” square pieces and then cleaned before used as a device lid. The cleaning procedure is as the following:[3]

a) Gently blow sample with N2 gun. Pay attention to particles along the sample edges. The sample has been laser cut. There is often debris along the edges.

b) Ultrasonic clean the sample for 1 to 2 minutes, or soak and hand wash, in a detergent solution to further remove debris along the edges. Example of detergent solution: Versa-Clean from Fisher Scientific, Catalog No. 04 – 342, 30:1 with water.

c) Rinse with DI water, IPA and dry with N2.

d) Transfer sample into glove box and preferably leave it there for a few hours before using to ensure a thorough degas.

All the devices were loaded into a thermal and humidity test chamber under the condition of 60°C and 93% RH for a TH test. For metal cathode devices, microscope inspection was performed after TH test to detect any metal corrosion. For PLED devices, the samples were either lit before and after the TH test, or lit continuously under ambient conditions. Visual degradation was recorded over the period of the tests. In all tests, devices sealed with glass lids accompanied corresponding devices sealed with Alien barrier film.

[3] While this procedure worked well several times, we also observed that in some cases severe curling of the samples could occur after this cleaning process. For now, the process conditions that lead to sample curling are not understood.

Since all devices degrade to some extent, only comparison between those with barrier lids and the corresponding ones with glass lids are meaningful indication how effective the film is as hermetic barrier. Figure 102, 103, 104 and 105 show some of the results.

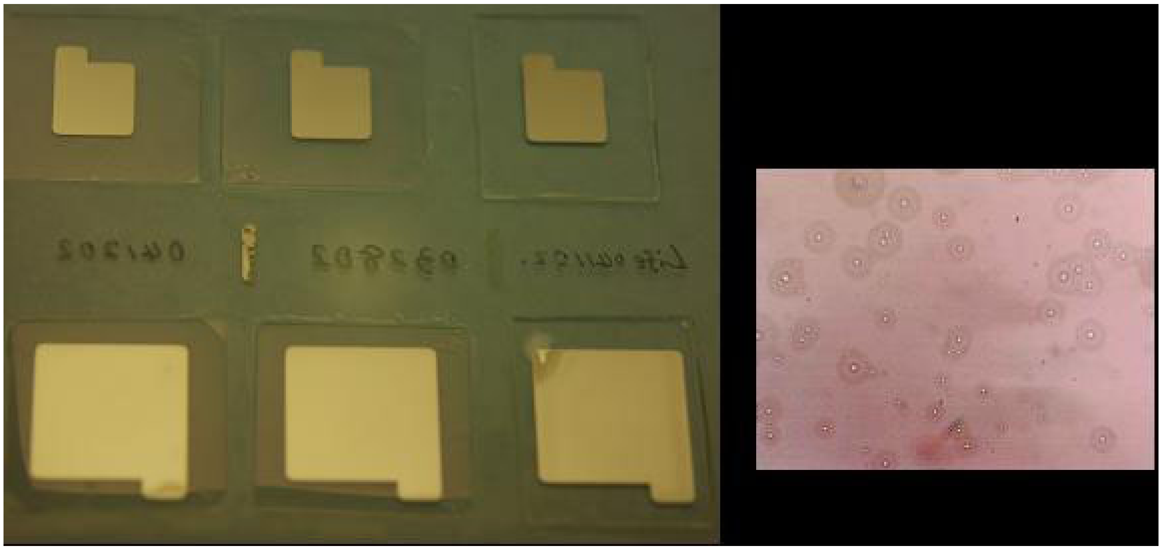


Figure 102 Left: Cathode metal (500 Å Ca + 2000 Å Al) after 4 weeks in TH chamber. Left two columns with Alien barrier as lid, right column with glass lid. Right: Cathode metal (500 Å Ca + 2000 Å Al) in ambient for 20 hours.

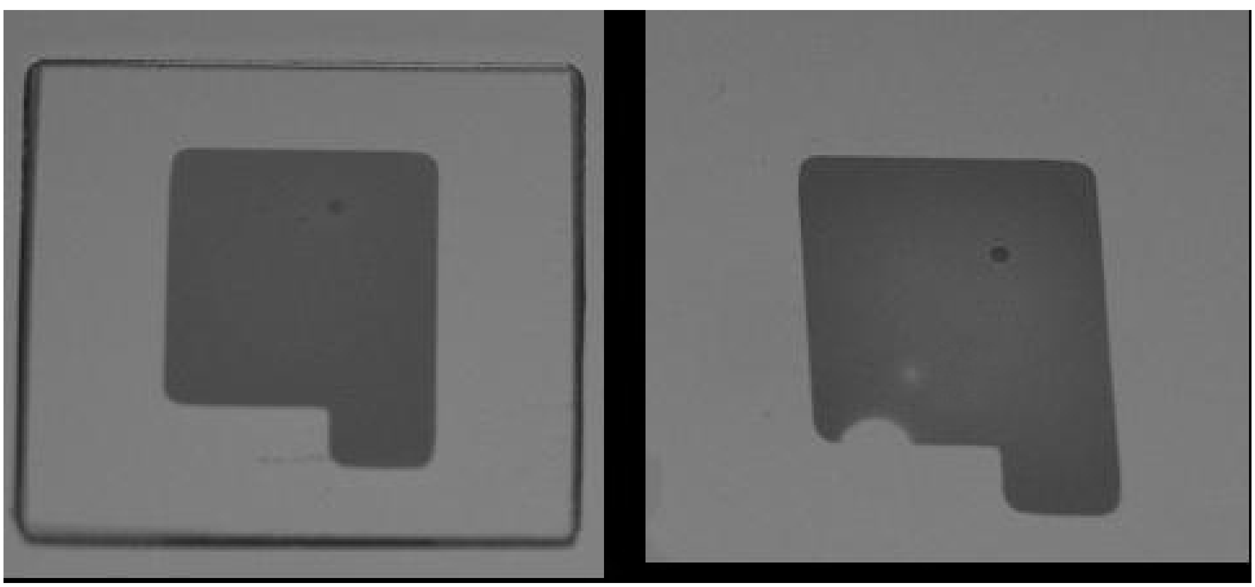


Figure 103.   Ca on glass after 7 days in TH chamber seal with a) glass and b) Alien barrier film.

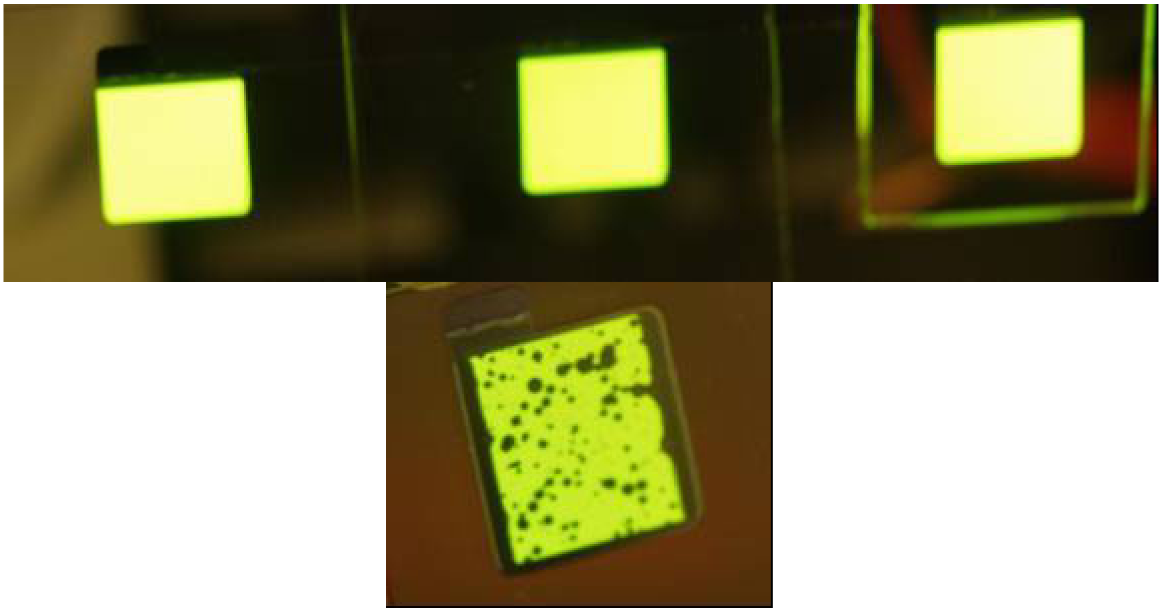


Figure 104. Devices after lit in ambient for 3 days. Top left and middle: sealed with Alien barrier film; Top right: sealed with glass lid; Bottom: sealed with a plastic lid.

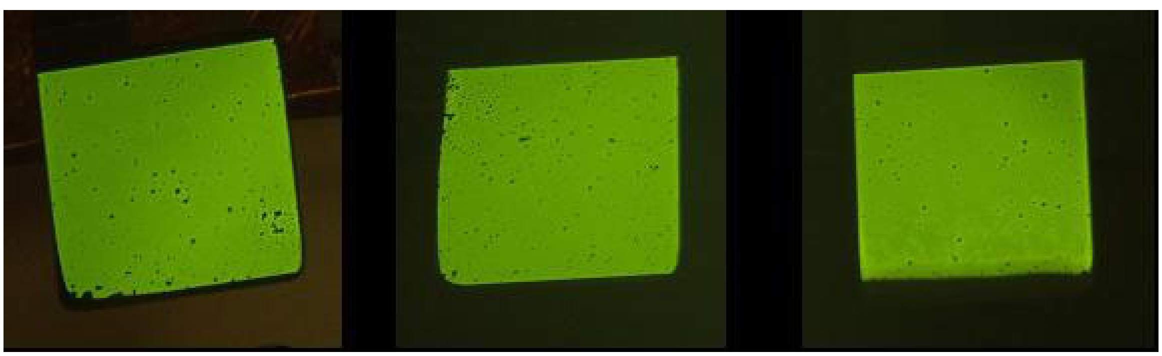


Figure 105. PLED devices with different lids after 1 week in TH chamber and 10 days in ambient. Left and middle: Alien barrier lid, Right: glass lid.

These early tests showed that the multi-stack SOG/SiO_2 film seemed comparable to glass as a hermetic barrier. However, it is difficult to draw a definitive conclusion from such a short period of testing. A consistent problem we faced during the limited period of time when we attempt to evaluate the barrier film was that our epoxy sealing process was not optimized. A sealed Ca film, which is believed the most sensitive test device, was often seen corroded even before it was taken out of glove box. Similarly, a PLED device often decayed severely in a relatively short period of time even when it was sealed by glass. The problem is believed to derive from a non-optimal epoxy which possibly attacked the cathode metal. We also believe that we used a non-optimal sealing process. These sealing problems prevented most of our PLED devices from having a long lifetime regardless of

lid material used. As a result, we were not able to perform an expended period of evaluation on the device to make a strong conclusion. Had the program continued, we would have worked with outside organizations to both improve our sealing and testing protocols, as well as develop an independent assessment of the technology.

In order to make sure that the barrier coating on PET is suitable for flexible display, a bend and twist test was also performed. Samples went through 500 times back and forth bending with 34.5 radius and twist +/-15° for 1000 times. No cracking was found in the film.

10.5 Discussion

It is well known that fabricating thin film hermetic barrier in general faces severe challenge, mainly because it is highly susceptible to particles or pinholes and requires highly condensed materials. The SOG/SiO_2 multi-stack has some built in self-correcting effect in that respect, in that the SOG can full fill pinholes or planarize particles in SiO_2 film. Nevertheless, there are still many factors that are difficult to control and contribute to high oxygen and water permeation rates:

- Plastic substrate used as substrate. A commercially available plastic sheet is typically full of pits and particles. Figure 106 shows a Wyko optical image from a cleaned PET surface. Its total roughness is 1.7 um. Apparently, anything that is not planarized by the first SOG layer, which is typically 0.5 um thick, will cause a defect in the subsequent SiO_2 layer. To find a plastic film without such defects is near impossible, even though one can expect some improvement from a specifically developed film.
- Rapid condensation of SOG solution. Condensation of a low curing temperature SOG precursor can take place during spinning, resulting in numerous small particles embedded in the dried SOG film. This problem has been overcome in semiconductor industry where a specially designed spinner with a well-controlled environment is utilized. With the reality limitation, we were only able to spin SOG in an existing photo resist spinner. After a great deal of effort spent on improving the spinning procedure to reduce particle formation, we were able to eliminate most but not all particles from this process
- Porosity in SOG film. To produce a highly condensed SOG film, an optimum spin condition plus a high degree of curing are required. With a less desirable spinning environment and low temperature cure, our SOG film is expected to have a relatively low density. In addition to the above difficulties, as does everyone else, we also face typical such production problems as airborne particles and those from SiO_2 deposition.
- Finally, the combination of dry (low pressure) and wet (higher pressure) processing poses a challenge in the practical implementation of these structures as a cost-effective barrier material.

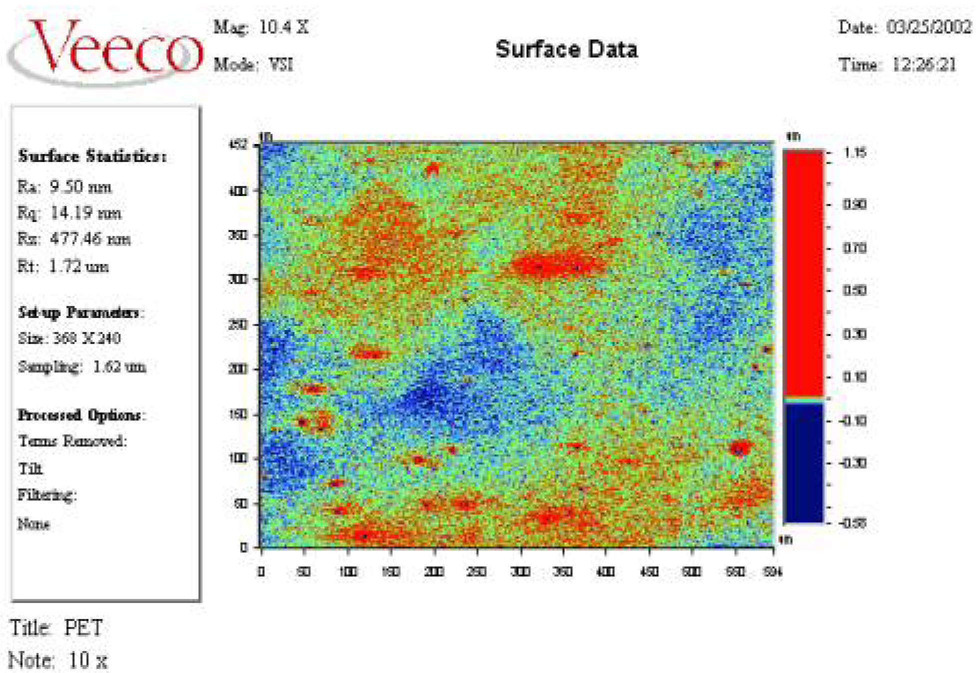


Figure 106. Optical image of a cleaned PET surface

10.6 Development Pathway

Based on the above discussion, there are several avenues for future work:

- Develop a reliable qualification test for the barrier properties of the composite. This would include both a test for coating the plastic film (i.e., underneath the PLED device) as well as a top "lid" test.
- Examine the structure-property relationships of the SOG, and curing conditions of the SOG, for these barriers. Factors include:
  - The chemical structure of the SOG
  - Blends of different SOGs
  - Catalysts
  - Thermal curing processes, including convection and IR heating
  - Possible radiation or photochemical curing processes
- Examine the process and material set for the sputtered glass
- Determine the effectiveness of the barrier as a function of layer thickness and number of layers. Include environmental stress factors in this evaluation
- Keep eventual manufacturing processes under consideration.

10.7 Conclusion

A multi-stack of SOG/SiO2 was fabricated as a hermetic barrier film for PLED devices on plastic substrate. The film is compatible with subsequent PLED processing and can easily be patterned for electric contacts. Preliminary life and reliability test on PLED devices and cathode metal show that while the system is not currently a total solution for sealing PLED on plastic, it is promising, and warrants additional investigation.

11. SUMMARY

The goals of this flexible display initiative was to enable a new means of constructing polymer LEDs on plastic substrates. The innovative use of NanoBlock ICs and Fluidic Self Assembly (FSA) broke new ground in demonstrating the integration of silicon with plastic substrates.

Many challenges were overcome in demonstrating basic functionality, but many lessons were also learned along the way. In particular, the idea of depositing hundreds of thousands of NanoBlock ICs to drive a million-pixel display was found to be exceedingly difficult. While the basic concept is feasible, for today's NanoBlock ICs the cost of silicon for a megapixel display is not competitive with existing TFT technologies. Additionally, there is a substantial engineering component in driving up the yield of interconnects to make a fully functioning display.

Despite these difficulties, NanoBlock ICs can still have their place in flexible displays. At the time of termination, Alien was driving towards row and column passive NanoBlock IC drivers. These drivers could be deployed on a flexible strip to be bonded to either glass or plastic displays, or could be embedded within a flexible substrate. Such an approach would allow these drivers to leverage off the PLED development efforts of other organizations. Additionally, such an approach could lead to tiled passive displays, a means of achieving high pixel counts in a large form factor display.

11.1 NanoBlock IC

Though respectable uniformity of ±4.0% of output currents of Jade NanoBlock IC was achieved on inter-batch basis, it was higher then simulated by a software T/SPICE. Similarly, the nonuniformity between the eight outputs of each NanoBlock IC as well as between the NanoBlock ICs within the wafer were also higher then than the results of the simulation. Thorough analysis of test data and additional tests are needed as discussed in greater detail in.

Another improvement needed for directly driven displays is the restoration of the clock signal within each NanoBlock IC (buffered clock). In the current design, the clock line runs continuously and feeds the clock signal in all NanoBlock ICs in parallel (thus only one pad is needed). The signal degrades as it travels along the narrow clock line due to transmission line effects (large RC product). The redesigned architecture would feed the signal in the input clock pad of the NanoBlock IC, signal then will be restored within the NanoBlock IC and exit from the output pad to be fed in the next NanoBlock IC. This way the slight degradation of clock signal along the short distance between the neighboring NanoBlock ICs will not cause wrong interpretation of the signal by the receiving NanoBlock IC.

The recommended improvements in ESD protection are discussed in section 5.8.2. Design changes are needed to increase the current ESD test failure level of 100-200 V.

11.2 Advanced NB Backplane with Barrier Layers

The difficulties of integrating the PLED structure with the NB backplane experienced during the Phase I were partially caused by the fact that the ITO itself did not provide adequate protection for the PLED materials from the underlying organic layers. The problems were mitigated to a great degree after the introduction of additional layer (SiO_2) that served as chemical barrier. While quite successful in providing an acceptable surface for PLED structure, its introduction resulted in more complicated structure and additional processing steps.

To simplify the structure and associated processes, we proposed to integrate a multilayer barrier layer within the structure and use a second multilayer barrier for encapsulation as well. Additional simplification will come from a plastic substrate with preformed receptor sites. Such substrates are expected to be available in the near future. By adopting this approach we will accomplish several goals; 1) fully separate the PLED structure from the organic materials underneath, 2) use the multilayer barrier layer for planarization purposes and 3) use the multilayer barrier layer to achieve a hermetic seal around the periphery of the display as shown in Figure 107. Such a structure will allow to build high quality PLED displays having long lifetimes (determined by properties of the barrier layers). To support production of such a NB backplane we need to develop the capability to remove the tilt of NanoBlock ICs by dry planarization and to etch vias through the Vitex barrier layer. Experiments are already under way to establish such capabilities.

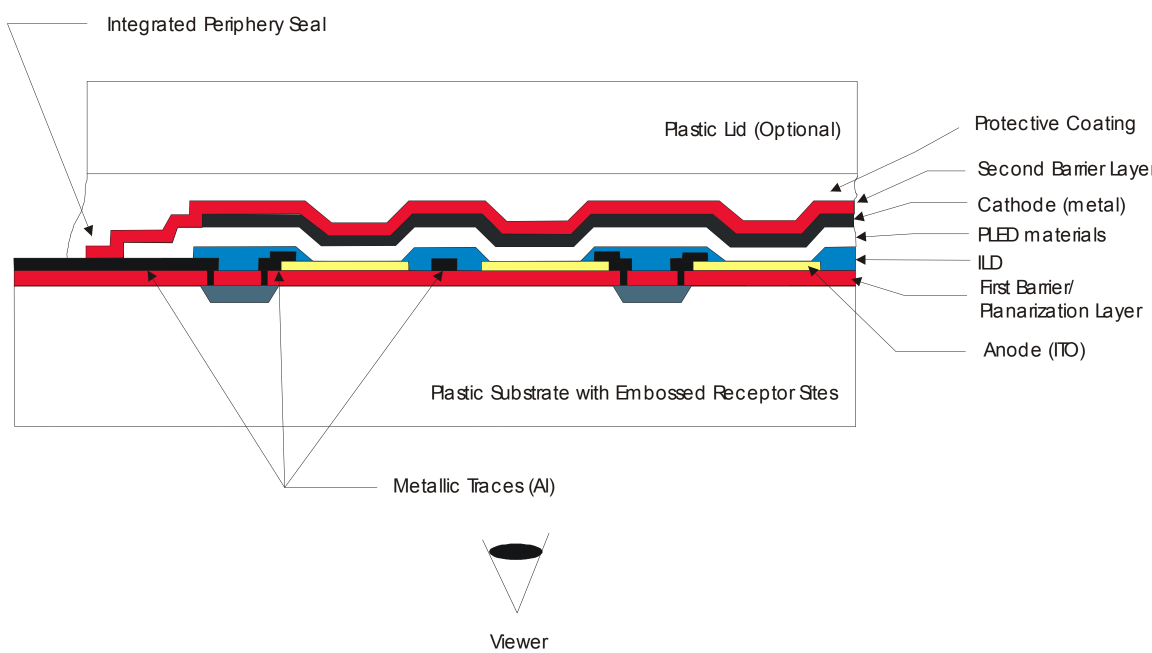


Figure 107 Advanced NB Backplane with integrated multilayer barrier

11.3 Row and Column Drivers

Though high resolution displays are possible with the approaches described above, high resolution, direct driven displays built on the NB backplane will not be cost competitive with stan-

dard active matrix approach (p-Si) for a number of years. The primary reason for this high cost is the total cost of the silicon that would be deployed using today's design rules for NanoBlock ICs. Deploying hundreds of thousands of NanoBlock ICs and interconnecting them would also require substantial process development. While this is on Alien's long term development path, near-term development is aimed at different directions.

Our belief is that there are nearer-term approaches to achieve attractive high resolution displays with NanoBlock IC technology. An approach that is attractive on a number of levels is to develop NanoBlock ICs that can serve as row and column drivers for a passively-addressed PLED/OLED display. We can deploy these row and column drivers either as flexible electronic strips that can be attached to a display edge, or as embedded into a backplane. This approach is in line with Alien's commercial direction, and yet can provide displays with attractive benefits for defense purposes.

The advantages of this approach are numerous.

- Passive addressing allows for more rapid access to higher pixel count displays than a direct drive Nanoblock IC approach, at least for the near term
- The NanoBlock ICs for passive addressing will be deployed in one of two ways. The NanoBlock ICs can be assembled in a plastic strip, which can be attached to an existing display. Alternatively, the NanoBlock ICs can be integrated into a plastic backplane, and then an OLED or PLED display built on top of this architecture.
- These NanoBlock driver ICs will constitute an example of a practical "flexible" driver, as they will be deployed as small silicon elements in a plastic base.
- In a passive drive architecture, NanoBlock ICs can be designed in a "silicon core limited" approach, meaning that the silicon can be sized to meet the demands of the display drive. In most passive display drivers, in contrast, "pin limited" designs are common, as the minimum size of the driver is dictated by the practical aspects of silicon die placement and attach. A core limited design with NanoBlock ICs should provide significant cost savings over a pin limited approach with conventional ICs.
- In the "driver strip" approach, Alien NanoBlock ICs can be attached to displays made either within Alien, or by other manufacturers. As such, the advantages of Alien NanoBlock ICs can be combined with state of the art OLED/PLED technology from dedicated display companies. As such, compatibility with advanced display systems (with color, flexible substrates, enhanced durability and lifetime, etc.) is possible.
- The Alien passive NanoBlock IC drivers are versatile, able to output a variety of waveforms through external programming. Additionally, the approach is modular, in that the number of NanoBlock ICs in a driver strip can be chosen to match the number of rows and columns in the display. One set of IC designs will serve numerous display formats.
- Since the NanoBlock ICs can be distributed spatially across the strip, interconnection constraints are eased. Rather than rely on difficult and space-intensive fanouts, the NanoBlock ICs can be placed close to the lines they are driving. This will minimize resistivity drops across long traces, as well for a narrow bezel along the display edge.
- The NanoBlock driver ICs can also be embedded within the display. Since they will be deployed along display edges in a narrow line, interesting designs are possible. For ex-

ample, the NanoBlock ICs could be deployed under the edge seal of the display, leading to a "zero-border" display.

- Since the NanoBlock ICs can be embedded within the substrate, it should be possible over time to devise "passive tiled" displays in which small subsections of a display are driven passively, but are arranged spatially to give the appearance of a seamless high resolution display. Normally, passive addressing technology for PLED displays is limited to around 100 lines. While some tiling is possible today along display edges (dual scan approaches and the like), this allows for a most four display subsystems. In a tiled passive approach with embedded NanoBlock ICs, multiple passive displays could be deployed within a single sheet, allowing for line counts that today are only possible with expensive and rare polysilicon technology.

A tiled passive display was beyond the scope of the present Phase II work. The Phase II work, at the time of program cancellation, was developing the following capabilities:

- Design of row and column NanoBlock IC drivers for PLED displays
- Implementation of these NanoBlock ICs into driver strips
- The construction of working passive OLED/PLED displays. Displays were to be obtained from organizations outside Alien, and combined with Alien NanoBlock IC driver strips.
- The demonstration of passive PLED displays with NanoBlock ICs embedded in the display backplane. These displays would have been designed and built within Alien.

Completion of these tasks would set the stage for commercialization of NanoBlock IC driver strips. The passively addressed embedded backplane with NanoBlock ICs would also demonstrate the necessary technical feasibility for tiled passive designs. Assuming success, future work could pursue high-resolution tiled passive displays, either with commercial or defense-based partners and support.

This document reports research undertaken at the U.S. Army Natick Soldier Research, Development and Engineering Center, Natick, MA, and has been assigned No. NATICK/TR- 04/005 in a series of reports approved for publication.

APPENDICES

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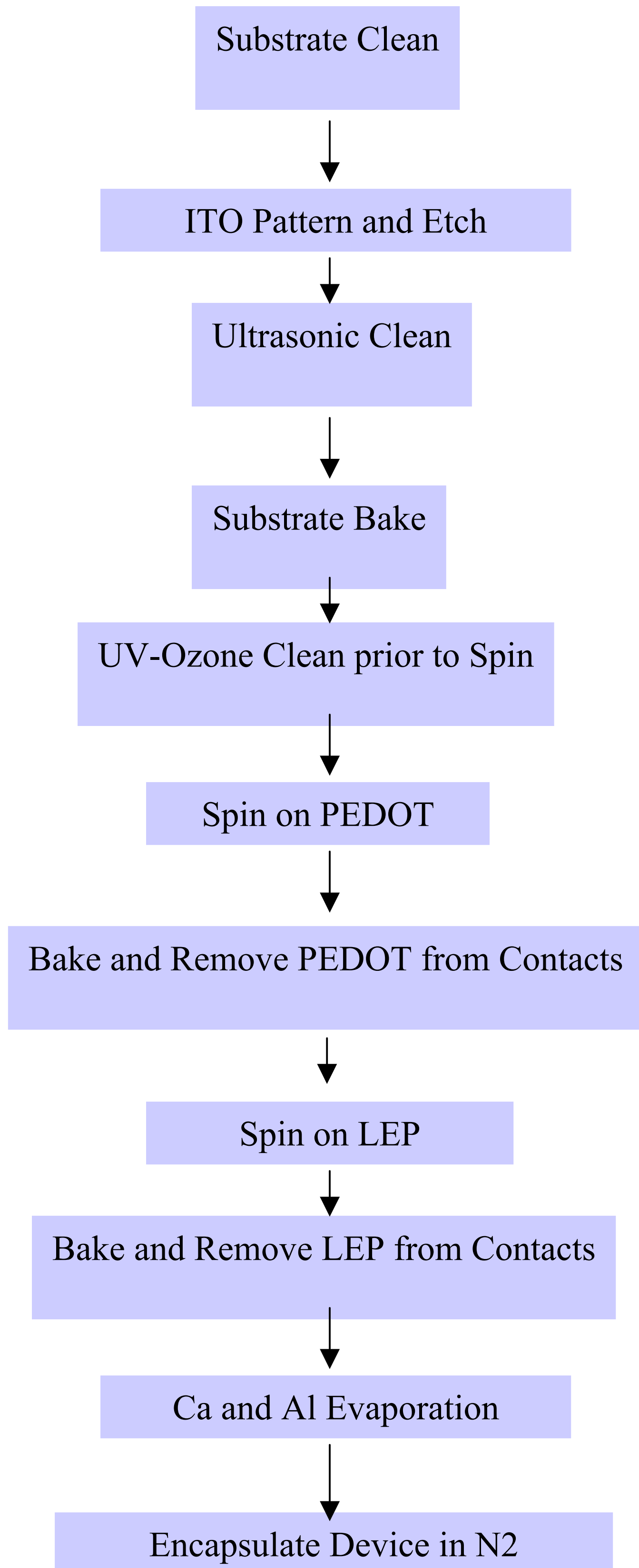
APPENDIX A.

Baseline Process for PLED Devices on Glass Substrate

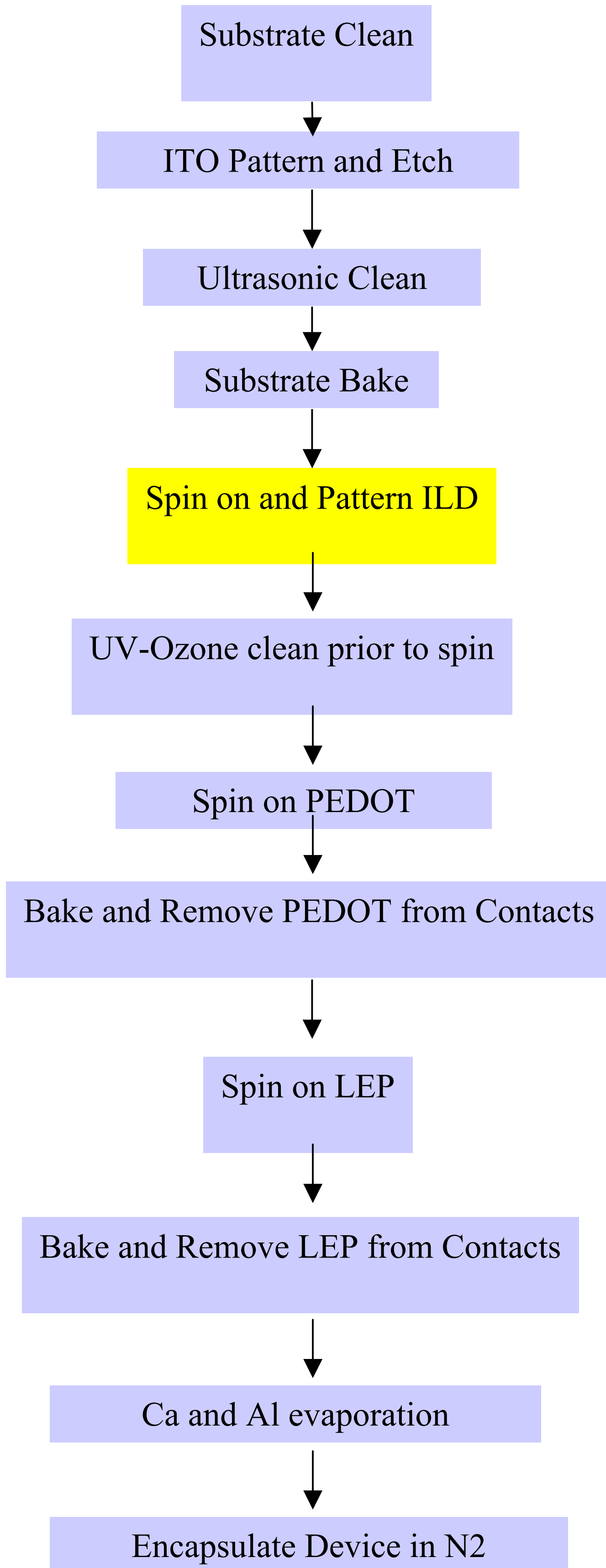
Baseline Process



APPENDIX B.

Logo Process

Logo Process



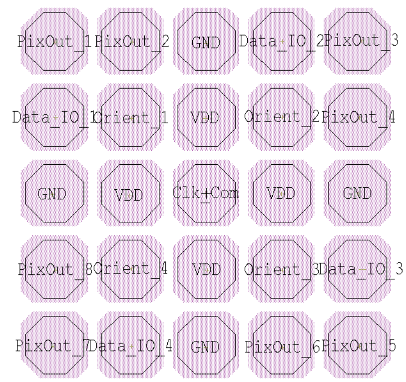
APPENDIX C.

Jade NanoBlock IC Spec Rev. B

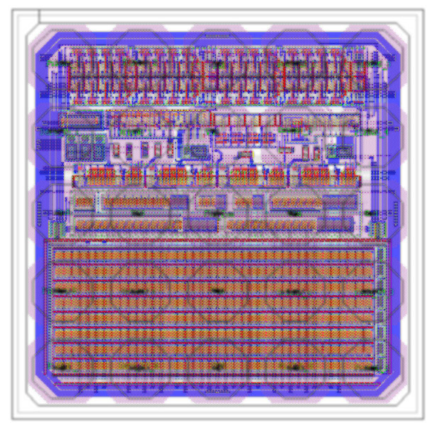
Jade is an ultra-compact, low power driver circuit for current driven displays such as Organic LED panels. This NanoBlock IC drives up to eight display pixels or segments. Gray scale is produced in the time domain using a four bit digital data format. The design is implemented in a 5V CMOS process and includes a compensation circuit to render the output current insensitive to CMOS process variations. Possible applications include segmented displays as well as direct driven active matrix displays and column drivers for passive matrix displays.

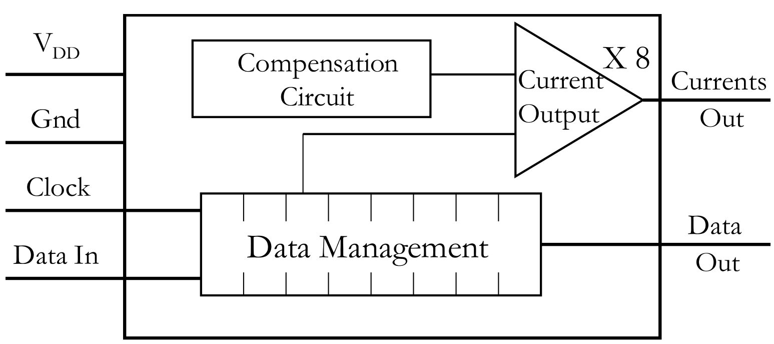
Specifications

Number of current outputs	8
Output current per channel	176 uA
Output current Uniformity	Currently ± 3 % (@ 5 V supply)
Quiescent current	20 uA (all OLEDs off) max.1.5 mA (all OLEDs on)
Gray Scale	Time Domain Digital, 4 bit
Physical Size	350 um x 350 um
NanoBlock IC thickness	62 um
Number of pads	25
NanoBlock IC pad pitch	68 um
Input signals	V_{DD}, Ground, Clock, Data_In
Output signals	Output Current 1-8, Data_Out
Number of transistors	862
Process	0.5 um 3 metal, 1 poly CMOS
Supply Voltage (nominal)	5 V ± 0.5 V
Supply Voltage (abs. max)	6 V
Digital core operating range	3.0 V – 5.5 V
Typical clock frequency	1 MHz (10% duty cycle)
Clock frequency range	DC to > 10 MHz
Operating Temperature	0 C – 70 C

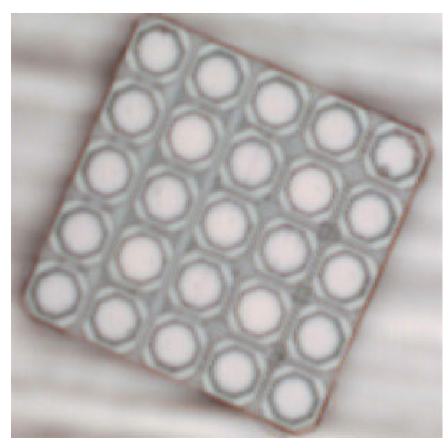


NanoBlock IC Pad Layout


NanoBlock IC Layout



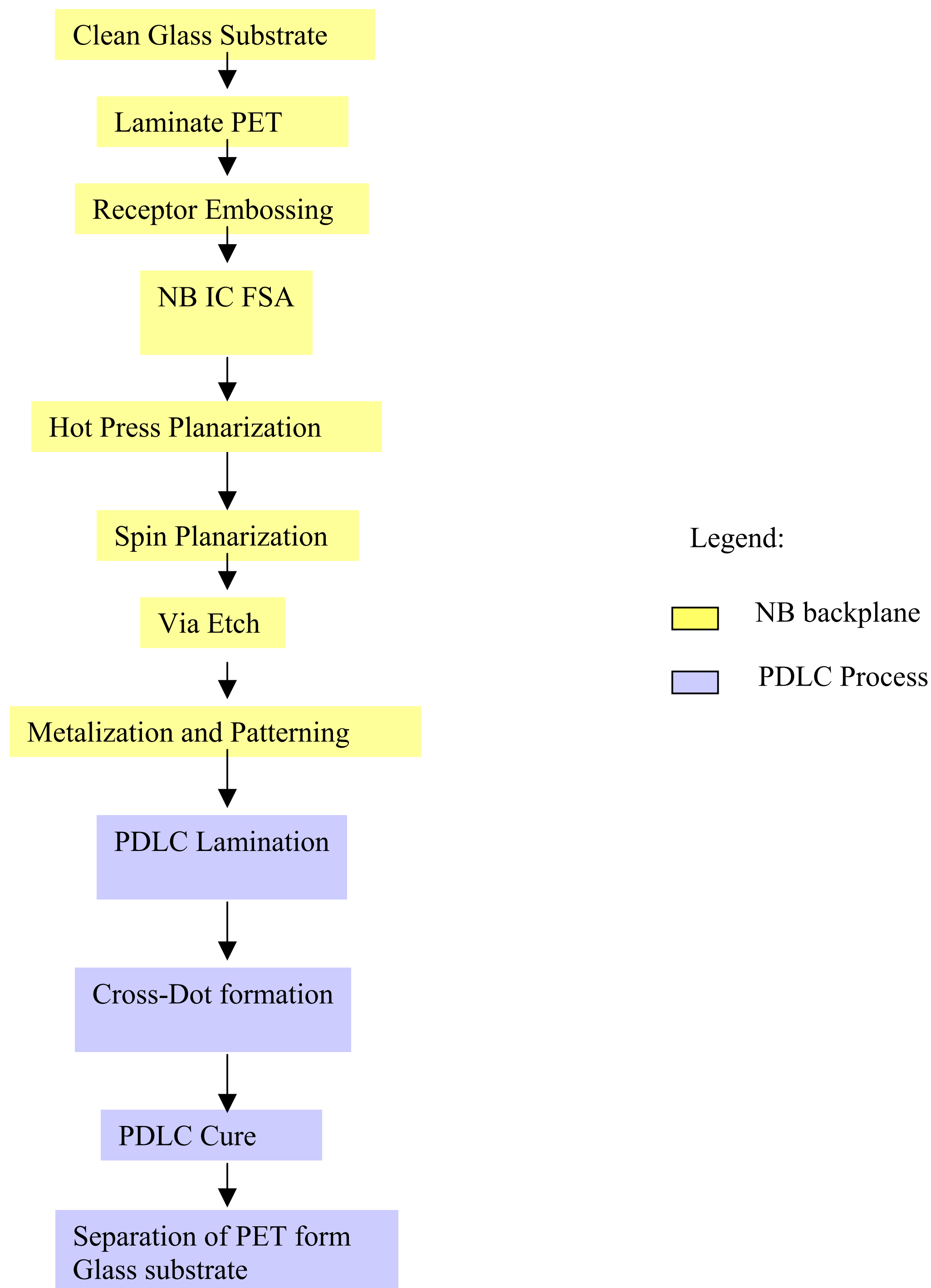
Jade Block Diagram


Released NanoBlock IC

APPENDIX D.

Standard Manufacturing Process for Integrated Alien Backplane

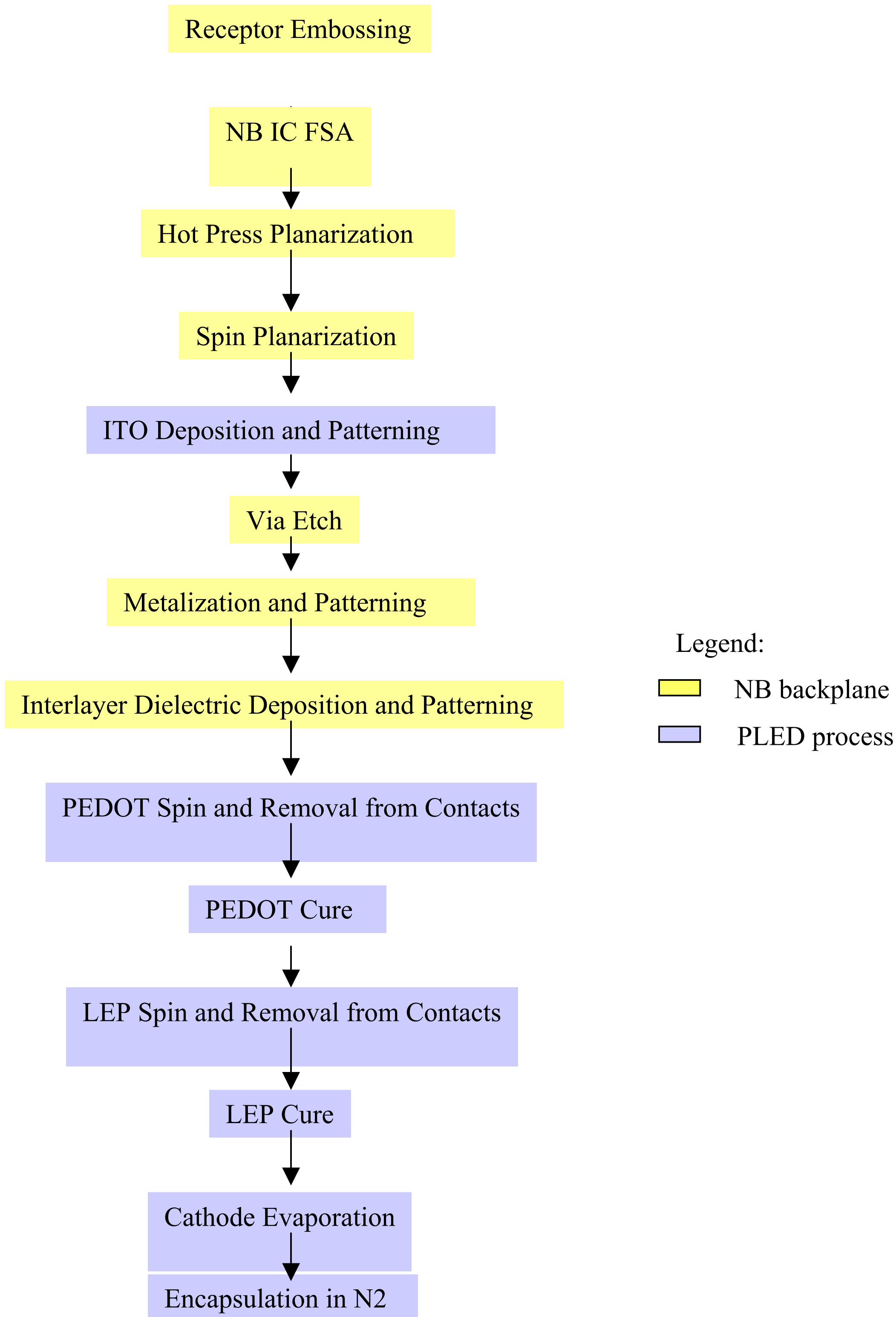
Standard Manufacturing Process Flow



APPENDIX E.

Initial Process for Integrated PLED Backplane

Initial TV-2 Process Flow



Receptor Site Formation

The process starts with a plain 4" x 4" x 1.1 mm glass substrate. As there are no alignment marks on the glass, the first step, namely the casting of the receptor sites into a thin polymer layer (embossing layer, NOA83H) spun onto the glass carrier, has to be referenced to the edges of the substrate. This casting process uses a silicon mold wafer generated with a 7" photomask and anisotropic etching of the mold wafer. The mask layer to generate the mold wafer is referred to as SUBSTRATE ETCH (gds II # 40). Only crude alignment is possible, but no further alignment is required. Every subsequent step is referenced to NanoBlock ICs in their receptor sites. Before the casting, the mold wafer is coated with very thin release layer. The casting is completed by cure at elevated temperature. The mold wafer is carefully removed after the cure.

Specifically, each backplane has two alignment marks, one on the left and one on the right, comprising a NanoBlock IC in its receptor site. The disadvantage of this method is that any missing, rotated or shifted NanoBlock IC in the alignment marks makes alignment of the subsequent process step very difficult, and usually results in pattern misalignment.

FSA

The next step is to assemble the NanoBlock ICs by FSA This is Alien's proprietary technology, so it must suffice to say here that NanoBlock ICs are flown in FSA solution along the tilted surface of the substrate and are seated in receptor sites already formed in the embossing layer. There is typically pre-FSA and post-FSA treatment, also of proprietary nature.

Planarization

The surface of the NanoBlock ICs are typically recessed several microns below the surface, and to avoid both wire discontinuities and shorting NanoBlock IC pads together, an interlayer dielectric is required. Uniform and controlled layer thickness in turn is critical to optimized PLED efficiency. If optimum efficiency cannot be attained, most of the benefits of direct drive – low power consumption and longer PLED lifetime - are lost.

When NanoBlock ICs are assembled into receptor sites, they are frequently tilted slightly. The next step therefore consists of a press planarization process. The planarization polymer NOA83H is coated over the assembled NanoBlock ICs and then pressed flat with either a silicon wafer or a quart plate, both coated with a release layer. This step assured level NanoBlock ICs but results in a somewhat rough surface after its cure in oven. Therefore, a final spin coat with the same material NOA83H is performed. The top polymer layer also known as spun-on planarization, is then cured by UV radiation.

Deposit and Pattern PLED Anodes

PLED anodes consist of Indium Tin Oxide (mask layer "ITO", gds II # 70). This transparent conducting electrode material is sputter deposited onto the planarization film and then patterned. This is the first patterning step after receptor site formation and NanoBlock IC FSA and therefore has to align to the filled NanoBlock IC receptor sites in the alignment marks. The

ITO mask features a wire mesh matching the spaces between the NanoBlock IC pads. The ITO is patterned by spinning on a positive tone resist, patterning it and wet etching the ITO. The resist then needs to be stripped in organic solution known as SafeStrip.

Pattern Vias through Planarization

The third patterning step after the receptor site formation and the ITO patterning is to cut vias through the planarization layer down to the NanoBlock IC pads that are to be contacted (DISPLAYVIA, gds II #71). For this purpose, a positive tone resist is spin coated onto the planarization layer and exposed where holes through the planarization are desired. After development, the resist is hard baked and serves as a etch mask for a Reactive Ion Etch through two underlying cured planarization layers (press-planarization and spin planarization). The residual etch mask is then stripped.

This patterning step can reference either the NanoBlock IC alignment marks or a patterned ITO structure. We chose to reference to the NanoBlock IC only. Note that the size of the via holes patterned in this process (24 um) is substantially larger than the mask feature size (15 um).

Deposit and Pattern Interconnect Metal

The next step is to deposit and pattern the interconnect metal (DISPLAYMETAL1, gds II # 72) between NanoBlock ICs and the PLED anodes (ITO). For this purpose, aluminum is blanket deposited (sputtered). Wires are formed by patterning a positive tone resist and wet etching. This step uses an etchant that stops on the ITO.

The alignment references DISPLAYVIA alignment structures. There are two DISPLAYVIA structures, a cross and a via hole, with a corresponding smaller cross and crosshairs in the DISPLAYMETAL1 mask.

Deposit and Pattern Interlayer Dielectric

The aluminum interconnect structures are thicker then the Light Emitting Polymer and the PEDOT Hole Transport Layer. Due to the sharp interconnect metal steps, the subsequent LEP and HTL spin coating steps would result in very non-uniform polymer films, and therefore PLED structures with substantial variability in its performance across the substrate. This problem can be addressed by coating the interconnect wires with a 1 um – 2 um thick, photo-imageable interlayer dielectric (ILD), with openings patterned into the ILD to expose the ITO anodes. The ILD (DISPLAYVIA2, gds II # 69) also substantially reduces the capacitance of the clock and data lines as well as the risk of electric shorts between Cathode Metal (see below) and interconnect wiring. Shipley photoresist 1813 was successfully used as ILD during the duration of the program.

The ILD mask can be aligned to the NanoBlock IC alignment marks, to ITO features and to DISPLAYMETAL1 features.

PEDOT and LEP Layers

After ILD patterning, the hole transport layer (PEDOT) and the light emitting polymer are deposited by spinning from solutions. We used a commercially available PEDOT form Bayer, which is water base solution with 1.5 % of solids. The LEP is typically a green polymer from Dow Chemical (Green B or Green K), which is dissolved in xylenes with concentration around 1%. The entire polymer LED (PLED) structure is about 200 nm thick. Before the thermal cure, the PEDOT and LEP are mechanically removed from the aluminum connecting pads. Typically the layers are cured on a hot plate at elevated temperature for an hour or so.

Deposit Patterned Cathode Metal

Next the cathode (CATHODE METAL, gds II #68) is deposited by thermal evaporation of thin (~ 10 nm) calcium layer for work function matching, followed by aluminum evaporation to provide metal conductor with good wok function matching to calcium. The aluminum layer also serves as encapsulation for the calcium layer. This also renders the cathode more highly conductive and less brittle. This two level metal structure is deposited through a shadow mask.

Alignment is carried out mechanically as the substrate is seated in a nest (depression) in the shadow mask. This coarse mechanical alignment was deemed sufficient for the purpose of the program.

Encapsulation

While more elaborate encapsulation techniques were available, for reasons of simplicity we decided to laminate a glass lid using an inert type of UV curable epoxy OG 114. Thus the substrate was transferred into a glove box through evaporator's exit load lock to prevent any exposure of incomplete device to oxygen and humidity in the air. The level of oxygen and water vapor was kept continuously bellow 2 ppm. The measured amount of epoxy OG 114 was then dispensed on the cathode and glass lid dropped on the blob of the epoxy. Capillary forces then distributed the epoxy along the device surface to the edges of the lid. The epoxy was cured by UV radiation. The typical thickness of the cured epoxy layer was 30 μm. After completion of the curing process the device was taken out of the glove box for evaluation.

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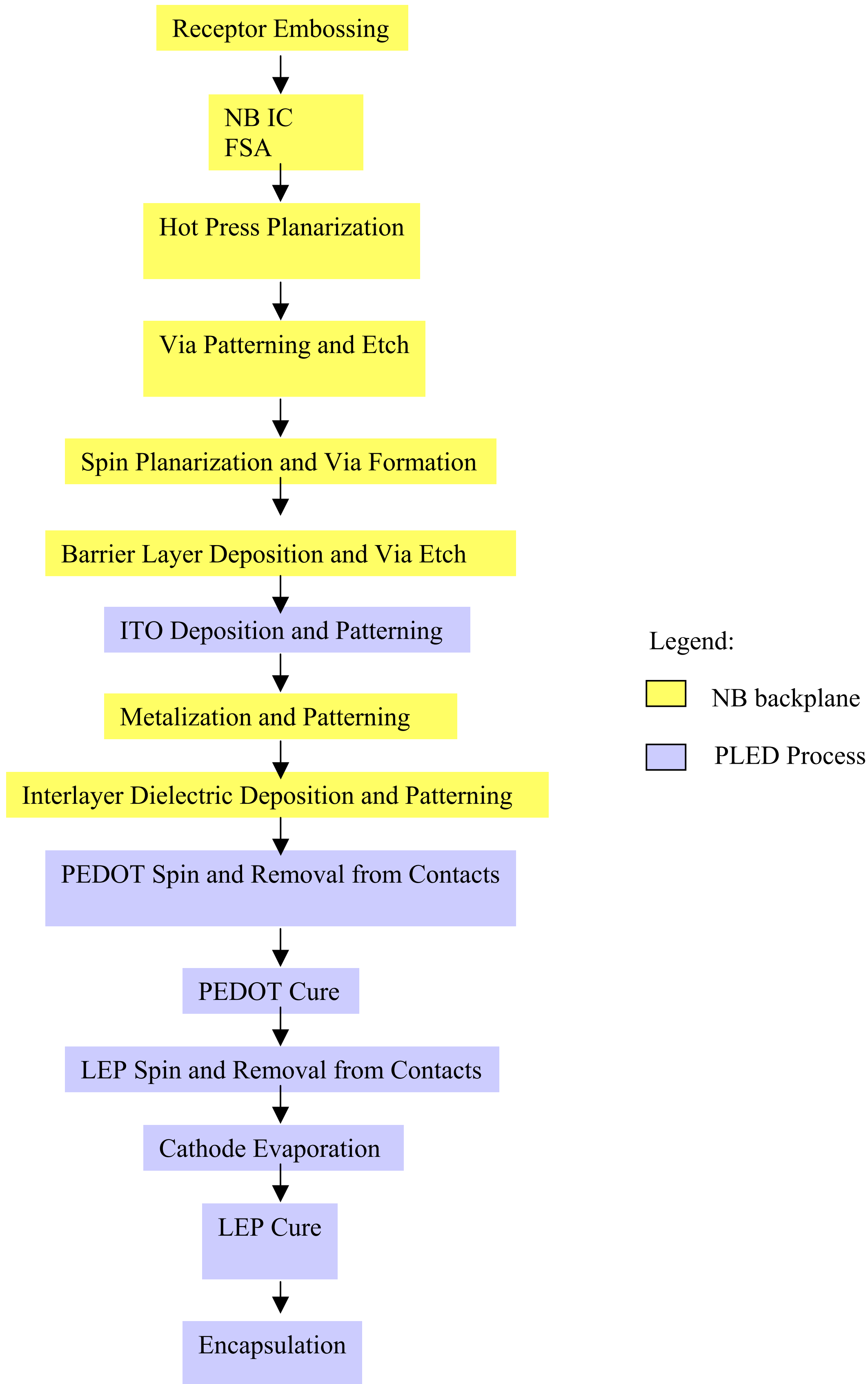
APPENDIX F.

Final Process for Integrated PLED Backplane

Final TV-2 Process Flow



Instead of describing the whole Final TV-2 Process, which shares many steps with the Initial TV-2 process, only the major changes are listed here:

1. Casting (embossing) material has been changed from NOA83H to Epoxy OG112-4

2. Press planarization material has been changed from NOA83H to Epoxy 169

3. Spin planarization material has been changed form NOA83H to SU8 negative photoresist

4. Via dry etch is done after press planarization (not after spin planarization)

5. Additional step: forming larger vias in SU8 layer directly by photolithography (no etch)

7. Additional Step: deposition of SiO_2 barrier layer by sputtering on the patterned SU8 surface

8. Additional Step: forming vias in SiO_2 barrier layer by dry etch.

All these changes were necessary to accommodate very stringent requirements of PLED technology, namely low surface roughness, chemical stability in wet processing, ITO adhesion to underlying plastic layer and final cleanliness of ITO anode before spinning the PEDOT and LEP layers.

Note: We call this a Final Process only with respect to the Phase I of the DARPA program. The availability of plastic films with NanoBlock IC receptors embossed already in it makes this process obsolete.

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APPENDIX G.

Schematics and PCB Layout for TV-2 Electronics

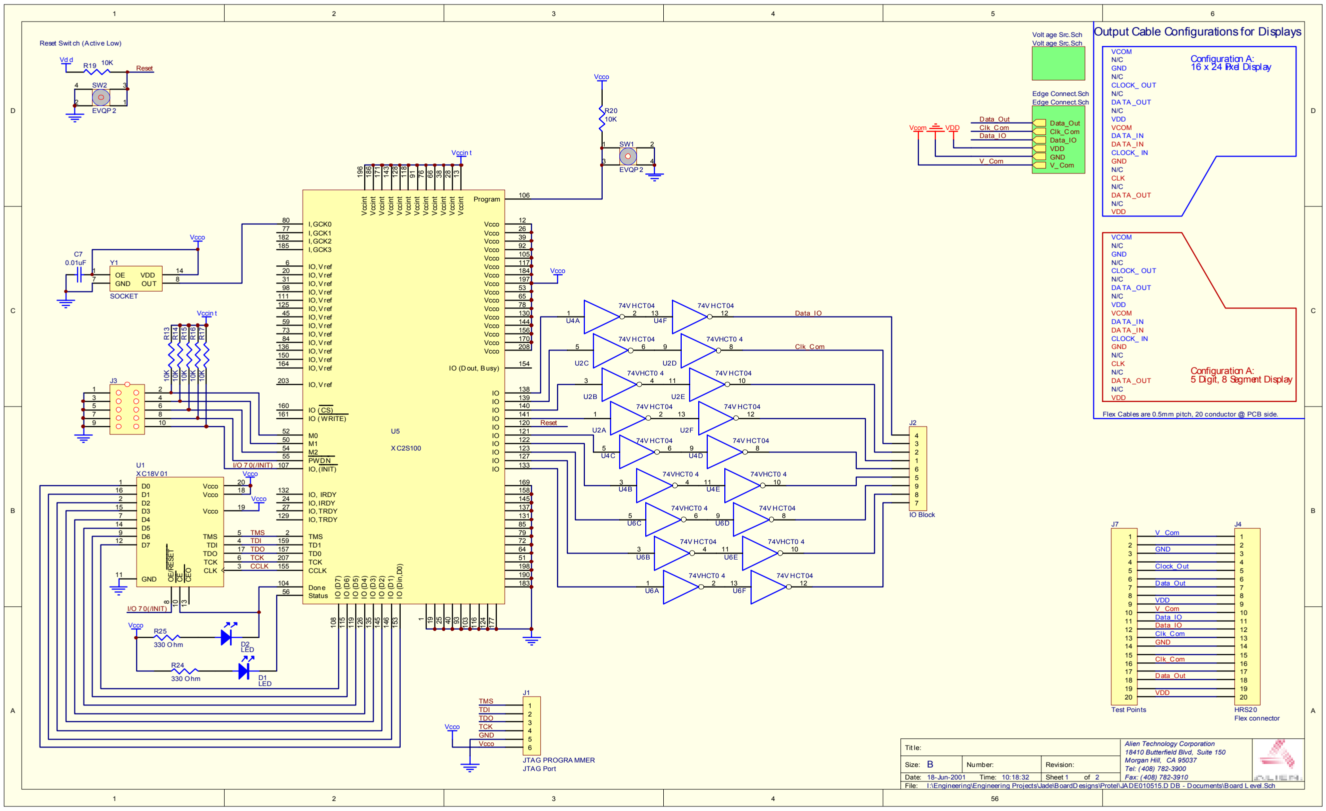

Figure G: 1 Microcontroller and Electronics

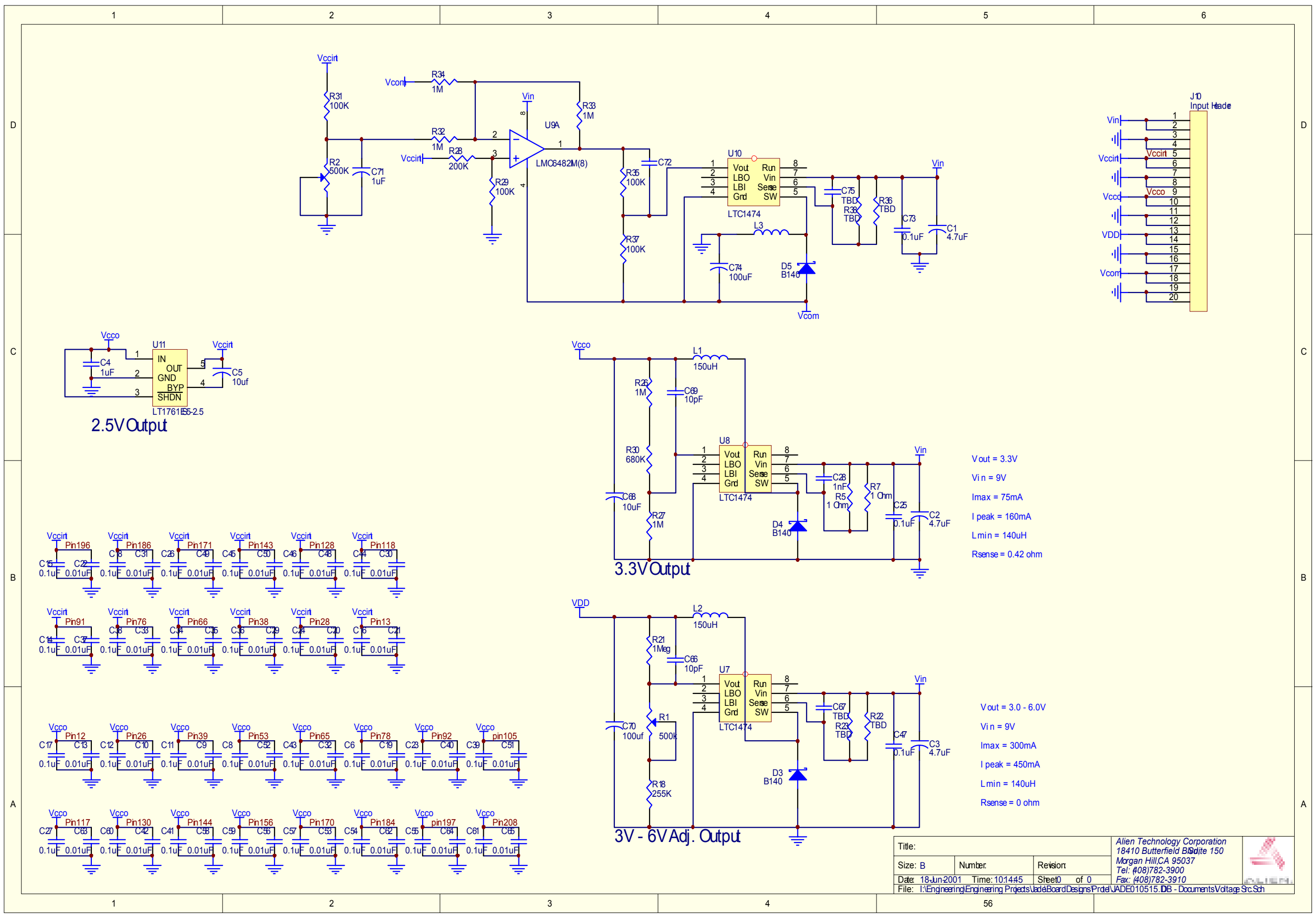

Figure G 2 Power supplies.

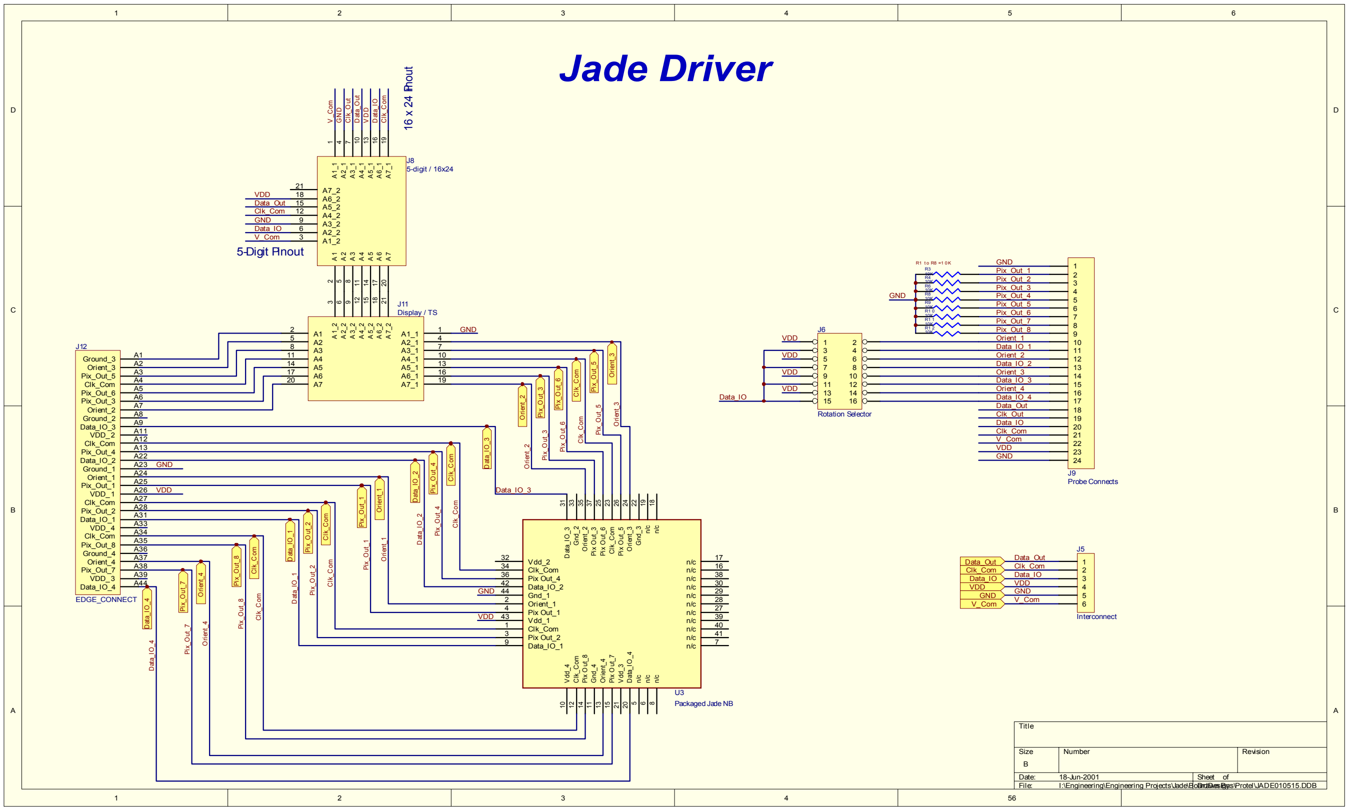

Figure G 3 Jade NanoBlock IC devices and connections

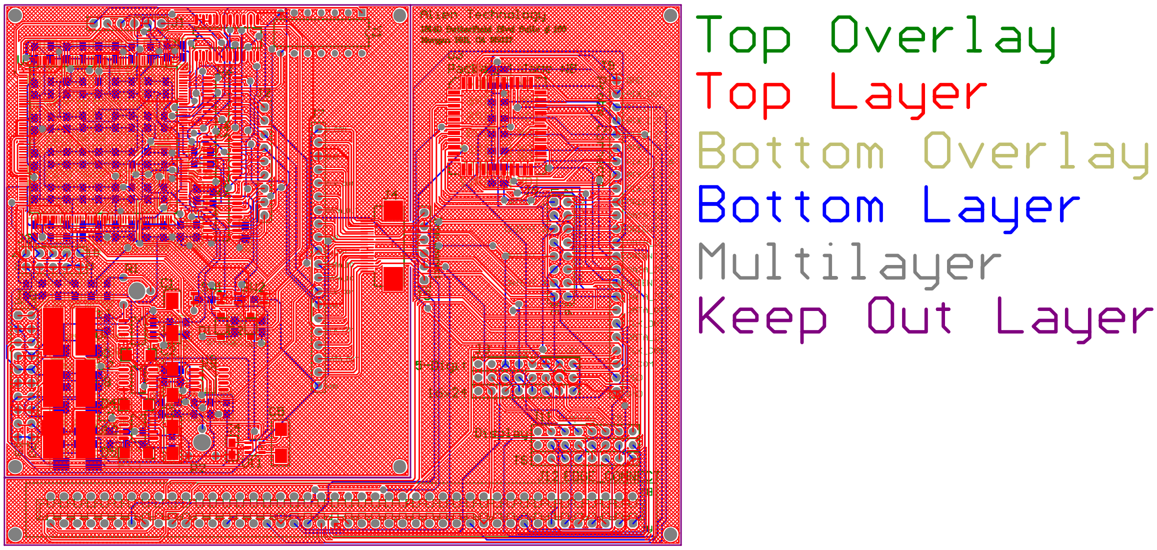

Figure G 4 Jade NanoBlock IC evaluation electronics – multi-layer composite

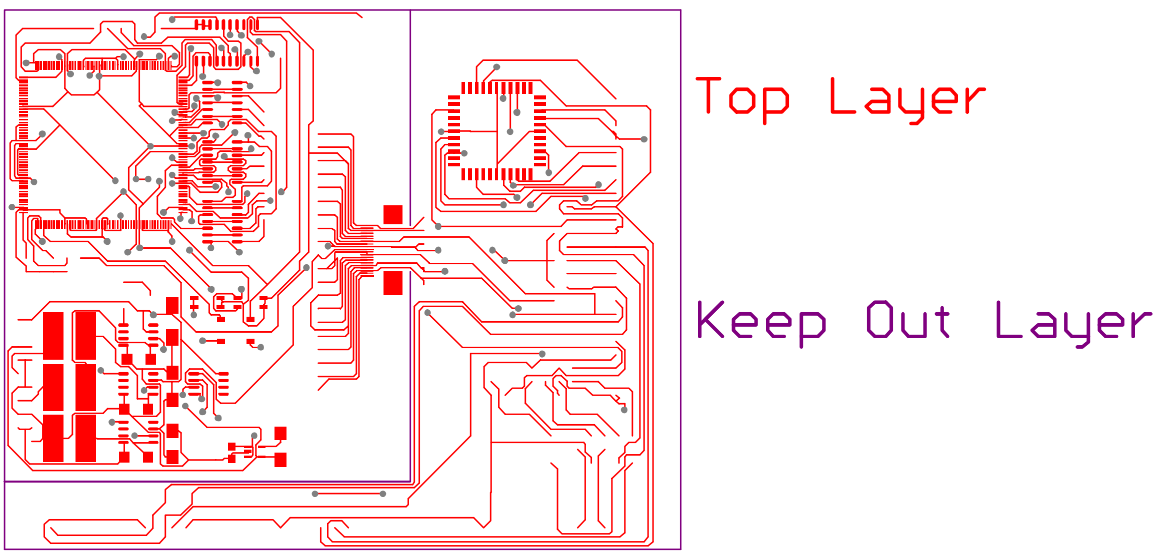

Figure G 5 Jade NanoBlock IC evaluation electronics – top layer (GND plane disabled)

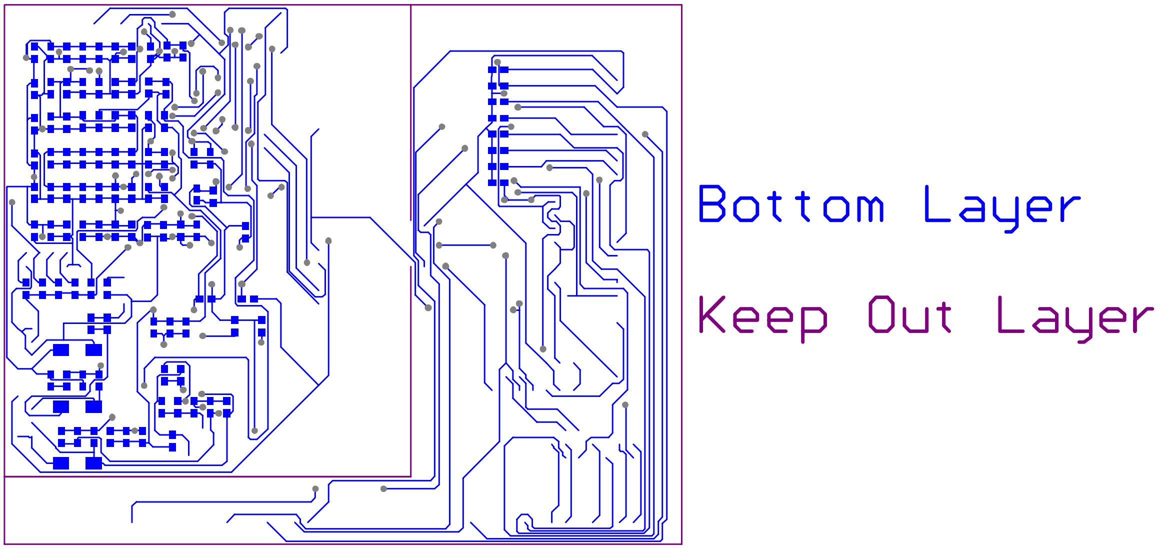

Figure G 6 Jade NanoBlock IC evaluation electronics – bottom layer.

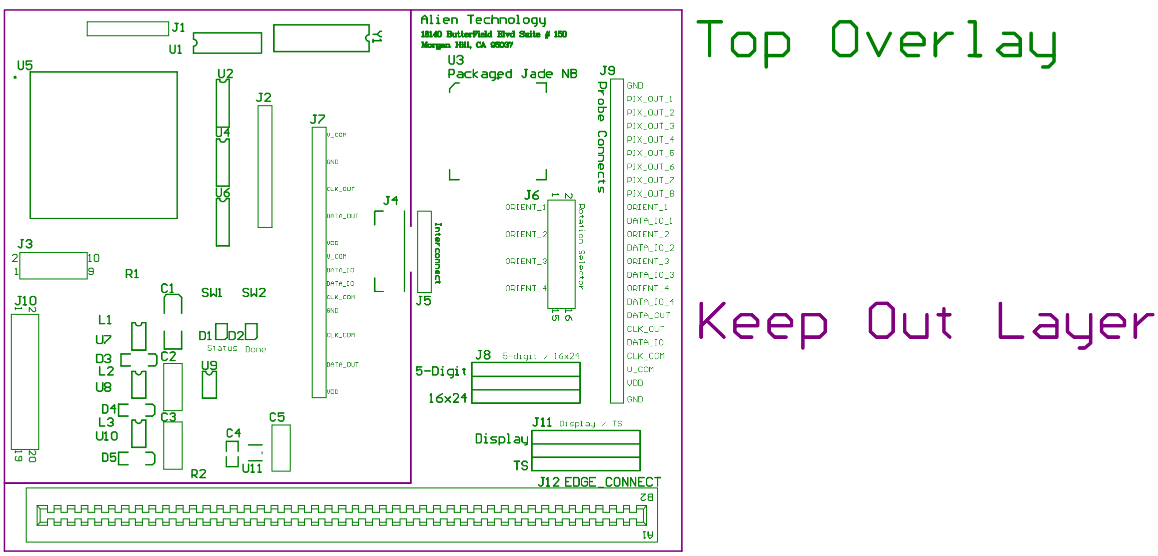

Figure G 7 Jade NanoBlock IC evaluation electronics – top overlay.

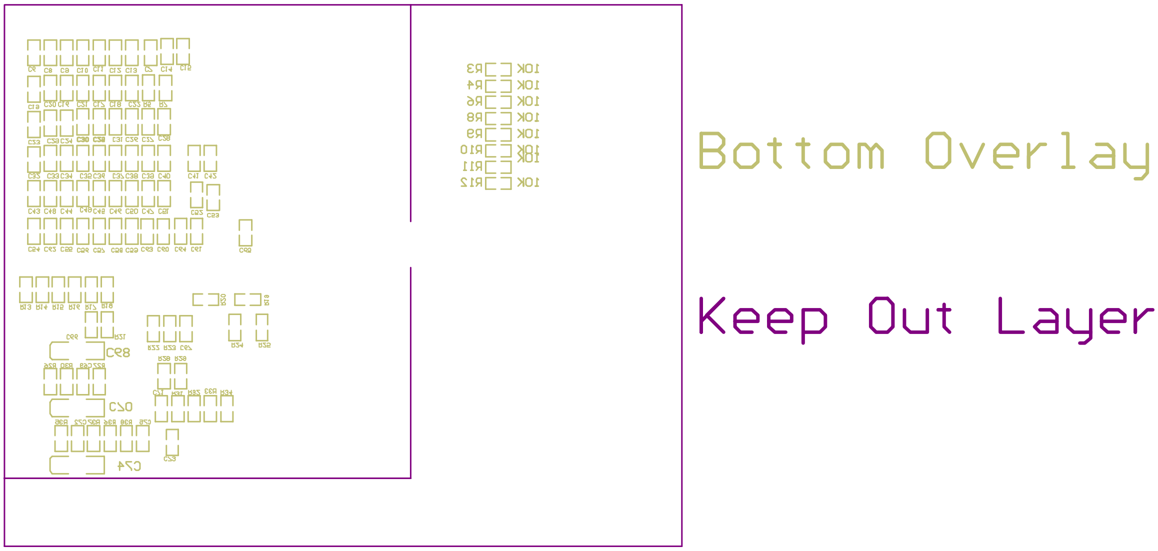

Figure G 8 Jade NanoBlock IC evaluation electronics – bottom overlay.

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APPENDIX H.

Experimental Data for Slot Die Coating

Table H 1 Liberty PEDOT Sheet Coating Trial Log

	Die Setup: 4" wide, 5 mil gap, Lip Configuration (unknown), approx. 6" wide die						
		center fed with vent out the top.					
	Pump System: IVEK, piston, resets stroke after each patch						
	Robot System: ADEPT						
						Wet	
	Sample #	Coating Gap	Speed	Dispense	Dispense	Calc. Thickness	Comments
		(microns)	(ft/min)	Vol (ul)	rate(ul/sec)	(microns)	
	1	25	6.7	300	66	19.2	Drying way too fast: glass placed directly on 400F
							hot plate
	2	25	6.7	150	33	9.6	
	3	25	6.7	150	33	9.6	Increased Acceleration Rate to get die at correct
							speed faster, lots of mottle from drying
	4	25	6.7	150	33	9.6	Repeat Of #3
							lots of mottle from drying??
	5	25	6.7	150	33	9.6	Started acceleration before plate so die was at speed
							before pump started
	6	25	6.7	150	33	9.6	Repeat of #5
							coating being scrapped off?? No repellencies = no coating
	7	25	6.7	100	22	6.4	
	8	50	6.7	300	66	19.2	coating being scrapped off

	9	50	6.7	150	33	9.5	drying mottle
	10	50	6.7	150	33	9.5	repeat of #10
							drying mottle - no coating in center (scrapped off)
	11	50	6.7	150	33	9.5	repeat of #10
							Non-uniform, coating scrapped off parts
							RESET OF COATING GAPS
w/Corona	12	40	6.7	150	33	9.5	3 dots in triangle from heating offset
v							45 seconds of corona using wire about 1/2" away from surface
							in a slow sweeping pattern.
v	13	40	6.7	150	33	9.5	tried piece of glass under drying glass to eliminate dots
v							LOTS OF DRYING MOTTLE
v	14	40	6.7	75	17	4.9	could not scratch coating -- Too Thin?
v							
	15	40	6.7	100	22	6.4	could not scratch coating -- Too Thin?
							no repellancies >> no coating
**	16	40	6.7	150	33	9.5	good quality, some repellancies
**	17	40	6.7	300	66	19.1	good quality
	18	80	6.7	300	66	19.1	2x gap
							good coating quality
**	19	80	6.7	400	88	25.4	good coating quality, some TD non-uniformities present
							(a band present in center)
	19a	120	6.7	400	88	25.4	Uneven coating side to side.
							Looks thicker than 19 (mis numbered?)

	20	70	13.4	400	176	25.4	2x speed
							the starting edge a lot more non-uniform, amplitude of
							wave pattern more than doubled.
	21	70	13.4	350	176	25.4	1/2 w/o corona. Corona improved coating quality >> less mottle
	22	70	13.4	250	176	25.4	
	23	50	13.4	100	66	9.5	lots of repellancies, high speed and low flow??
**	24	50	6.7	75	33	9.5	1x speed, lower number of repellancies
	25	50	6.7	75	33	9.5	repeat #24
							repellancies in evidence, still coated whole sheet
							while volume was cut in half
**	26	50	6.7	75	33	9.5	raise lips at end of run to eliminate thick spot
							---unsuccessful
							repellancies in evidence

Table H 2 FAS PEDOT Sheet Coating Trial Log

	Internal die shim: 1.5 or 2 mils							
	Lip land: 15 mils, 7 mil also available							
	Shuttle Acceleration after prime: 24 mm/sec^2							
	Prepump time: 5 seconds							
	Bead Prime (die stop at initial position): 1 second							
	Pump flowrate: 36 ul/sec							
	shuttle speed: 12 mm/sec							
	Coating Width: 195 mm							
				Wet	Dry	Meas.		
	Sample #	Coating Gap	Flowrate	Calc. Thickness	Calc. Thickness	Thickness	Comments	
		(mils)	(ul/sec)	(microns)	(A)	(A)		
Orgacon	1	5	36	15.4	1230.8		Pump stops 1 sec before die raised.	
	2	5	36	15.4	1230.8			good coating, 2 small repellancies
**	3	5	36	15.4	1230.8	1245.0	Pump changed to stop 2 sec before die raised	good coating, 1 center repellancy and a couple along starting and left edges.
	4	3	18	7.7	615.4		dewetting	Many large repellancies. Center and along edges. (glass broken)
	5	3	18	7.7	615.4		cleaned w/ acetone, still dewetting	all edges VERY craggy, large re-pellancies present
	6	6	60	25.6	2051.3		still dewetting, BAD side of glass	3 small repellancies, craggy start-ing edge
	7	5	60	25.6	2051.3		ethanol wash, little better, BAD side of glass	perfect middle, craggy starting and side edges.

	8	6	96	41.0	3282.1		Good side of glass, no dewet	perfect, except for staggered starting edge
**	9	6	96	41.0	3282.1	2069.0		**Perfect coating**
	10	5	96	41.0	3282.1			Perfect, except for small defect on left starting edge.
**	11	3	18	7.7	615.4	965.0	Good side of glass	Jagged trailing edge, and last half of right side edge. 3 large internal repellancies.
	12		27	11.5	923.1		repellancies again	**Brush pattern in the coating (reflective light with dark back-ground)**
**	13		27	11.5	923.1	1030.0	confirmed right side of glass	Perfect, one repellancy along right edge at end.
Baytron	14	5	36	15.4	1538.5		die lowered to 4 mils during bead initiation only	14A wipe marks come through - but no repellancies. 14B Mottle appearance with repellancies, no moon surface appearance.
	15		36	15.4	1538.5		w/ corona	Moon crater surface
	16		60	25.6	2564.1		w/ corona on half of coating	Still have surface appearance on both sides, hard to which side has corona
	17	6	60	25.6	2564.1		w/ acetone wash, and acetone to wipe lips vs dry rag, bead start at 3 sec from 2	**NO repellancies, but see the wipe marks**
	18	6	60	25.6	2564.1		back to 2 sec bead start	Good start, and then breaks up to all repellancies.
	19	6	60	25.6	2564.1		acetone wash	NO repellancies, but see the wipe marks
	20	6	90	38.5	3846.2		no acetone wash, coated good and then started breaking up	Large mottle pattern. Break ups initiated on the edges mostly.

	21	6	90	38.5	3846.2		w/ acetone wash	NO repellancies, but see the wipe marks, and/or large mottle pattern. Large trailing edge
	22	3	18	7.7	769.2		Perfect at coating	MD coating streaks, several large repellancies. Ragged edges. Some Mottle, good finish
	23	3	18	7.7	769.2		w/acetone wash	Very good trailing edge, some repellancies along edges only.
	defect			0.0				had several of these coating defects throughout trial -- need filter.

Table H 3   FAS LEP Sheet Coating Trial Log

Internal die shim: 1.5 mils							
Lip land: 7 mils							
Shuttle Acceleration after prime: 12 mm/sec^2							
Prepump time: 5 seconds							
Bead Prime (die stop at initial position): 2 second							
shuttle speed: 12 mm/sec							
Coating Width: 195 mm							
Coating Fluid: 1% LEP in Xylenes							
s.g. of xylenes = 0.86		s.g. of LEP = ?					
				Calc. Wet	Calc. Dry	Measured	
Sample #	Type	Coating Gap	Flowrate	Thickness	Thickness	Thickness	Comments
		(mils)	(ul/sec)	(microns)	(A)		
1	8x10 glass	3	25	10.7	918.8		
2	8x10 glass	3	25	10.7	918.8	938.0	
3	8x10 glass	3	20	8.5	735.0		
4	8x10 glass	3	16	6.8	588.0	801.0	
5	8x10 glass	3	12	5.1	441.0		
6	8x10 glass	3	8	3.4	294.0	418.0	
7	8x10 glass	3	4	1.7	147.0		
8	8x10 glass	3	2	0.9	73.5	344.0	
9	8x10 glass	3	35	15.0	1286.3		
10	8x10 Orgacon (#6)	3	25	10.7	918.8		
11	8x10 Baytron (#23)	3	15	6.4	551.3		
12	8x10 Orgacon (#7)	3	10	4.3	367.5		
13	6x6 glass(4 pieces)	3	25	10.7	918.8		Fluid through all the cracks onto back-side
14	8x10 w/ plastic	3	25	10.7	918.8		Set up level-ing
15	6x6 w/o leveling	3	25	10.7	918.8		Worked fine with plastic underneath
16	6x6 w/ corona cleaning	3	25	10.7	918.8		
17	6x6 Orgacon	3	25	10.7	918.8		No visible coating is-sues
18	6x6 Orgacon	3	15	6.4	551.3		No visible coating is-sues
19	6x6 Orgacon	3	10	4.3	367.5		First Streak
20	4x4 TV-1 Backplane	5	25	10.7	918.8		W01212e/20

21	4x4 TV-1 Backplane	5	25	10.7	918.8		W01212a/21
22	4x4 TV-1 Backplane	5	20	8.5	735.0		W01212f/22
23	4x4 TV-1 Backplane	5	30	12.8	1102.6		W01212d/23
24	6x6 glass	3	15	6.4	551.3	637.0	Tried adjusting gap, but table does not adjust w/o first leveling
25	6x6 glass	3	15	6.4	551.3		
26	6x6 glass	3	15	6.4	551.3		
27	skipped	3		0.0	0.0		
28	6x6 glass	7	15	6.4	551.3	834.0	
29	6x6 Baytron	7	15	6.4	551.3		
30	6x6 glass	11	15	6.4	551.3		No Coating
		9	15	6.4	551.3		No Coating
31	6x6 Baytron	3	20	8.5	735.0		
32	6x6 Baytron	3	10	4.3	367.5		Die hit glass

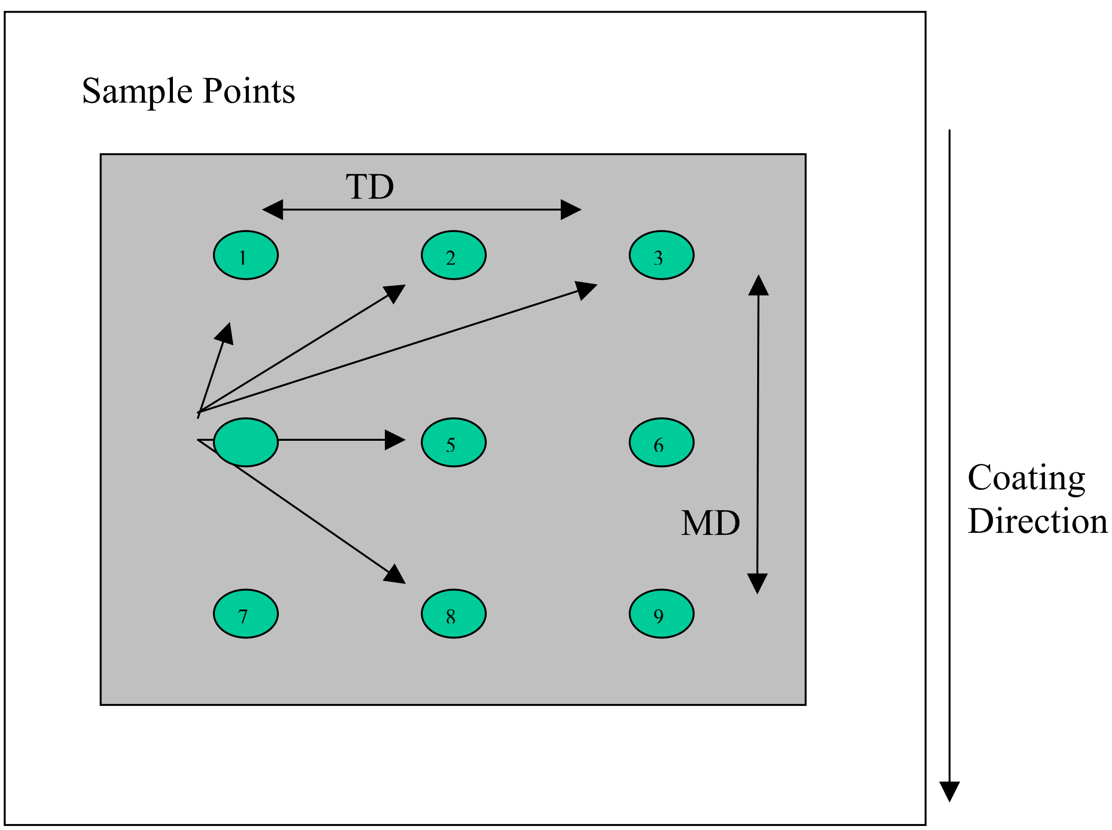


Figure H-1 Coat Weight Profile Measurement Points

	#24 6X6			#28 6X6			#4 8X10			#6 8X10		
	Left	Middle	Right	Left	Middle	Right	Left	Middle	Right	Left	Middle	Right
Top	700	505	650	700	700	916	865	905	1049	411	412	380
Center	597	546	608	814	669	1000	720	772	709	483	392	381
Bottom	629	711	790	989	814	906	731	741	720	350	463	494
	ave		637			834			801			418
	std dev		87.5			126.2			115.8			50.3
							4 mm ending edge			3 mm ending edge		

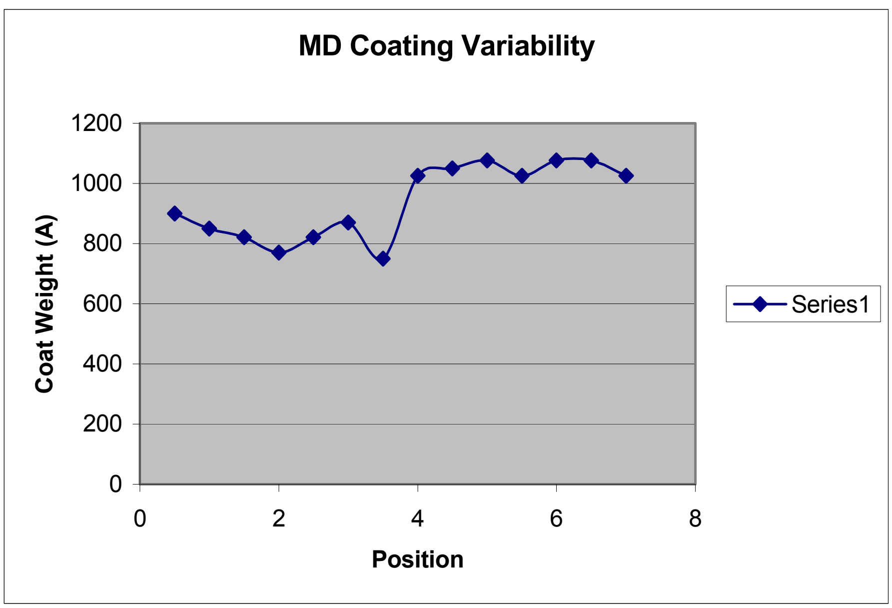
	#8 8X10			#9 8X10		
	Left	Middle	Right	Left	Middle	Right
Top	360	360	423	1452	1184	1328
Center	206	258	360	1410	1494	1545
Bottom	257	432	442	1617	1650	1669
	ave		344			1483
	std dev		85.4			159.7
	edge very sharp, 500 um wide			11 mm ending edge		
	2 mm ending edge					

Averages

Left	Middle	Right	Top	Center	Bottom
738	723	798	739	765	813

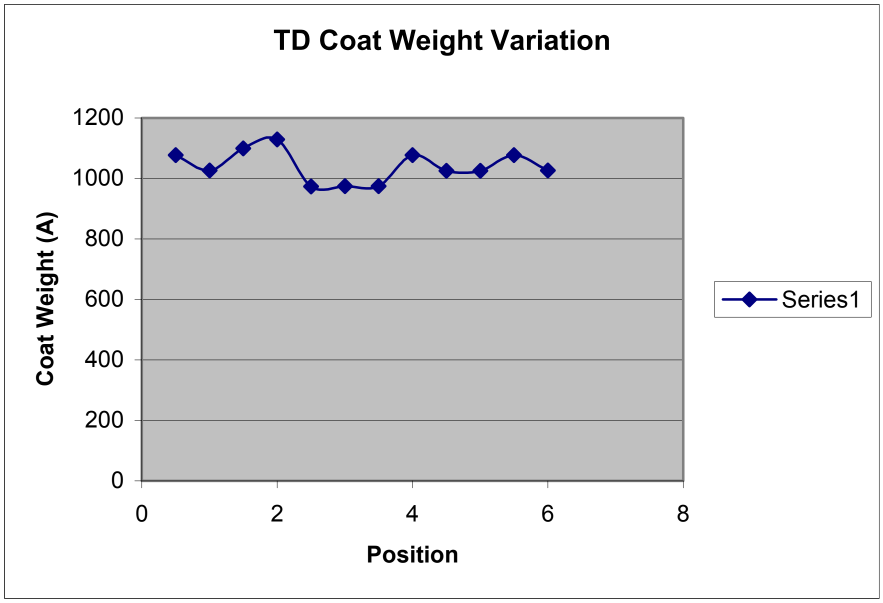
Coat Weight Profile on Sample #2

#2 MD down center	Inches	Coat Wt. (A)
Die Start	0.5	900
	1	850
	1.5	821
	2	770
	2.5	821
	3	870
	3.5	750
	4	1026
	4.5	1050
	5	1077
	5.5	1026
	6	1077
	6.5	1077
Die Finish	7	1026
avg		938.642857
sd		123.565994



#2 TD across middle

	Inches	Coat Wt. (A)
Left	0.5	1077
	1	1026
	1.5	1100
	2	1129
	2.5	974
	3	975
	3.5	975
	4	1077
	4.5	1025
	5	1025
	5.5	1077
Right	6	1026
avg		1040.5
sd		51.5866438
min		974
Max		1129
delta		155
% of avg		14.9%



Drying Conditions

Hot Plates

Initial Drying	Final Drying
60C	130C
1/2" offsets	10 minute minimum for backplanes

Cleaning Procedure

8x10 Glass Cleaning
Detergent wash/scrub
water rinse, with wand
IPA bath
N2 gun dry

6x6 Glass Cleaning
Detergent wash/scrub
water rinse (5 cycles)
acetone rinse top side
IPA bath
N2 gun dry

Luminence Date (after 1 month storage)

Sample #	Current (ma)	Luminence (Cd/m^2)	Cd/A
W01212A	10	85	0.85
W01212D	10	175	1.75
W01212E	10	118	1.18
W01212F	10	237	2.37

Table H 4 Frontier PEDOT/LEP Trial Log

1/22/01 Trial Date								
Die Setup								
	2 mil shim, 5" wide opening, 15 mil lips							
	Very low pressure recorded on gauge							
Dryer Setup								
	35 Hz on Z1 and Z2, 25Hz on air float, 180 F							
Pump Calibration								
`								
		Pump Set	Actual					
		(ml/min)	(ml/min)					
	water	10	6.6					
	Baytron	10	6	Lot K0009				
TRIAL DATA					Calc. Wet			
		Web Speed	Pump Set	Calc. Flow	Thickness	Die to Film	Vacuum	
Trial #	Solution	(fpm)	(ml/min)	(ml/min)	(microns)	gap (microns)	(in. H2O)	Comment
ROLL #1								
1	Baytron	20	15	9	11.6	75	3	increased vacuum to 3 to eliminate stripes
2	Baytron	20	15	9	11.6	50	2.75	Bead still holding at 6" vacuum
3a	Baytron	30	22	13.2	11.4	50	5	Min. Vacuum noted
TRIAL DATA					Calc. Wet			
		Web Speed	Pump Set	Calc. Flow	Thickness	Die to Film	Vacuum	

Trial #	Solution	(fpm)	(ml/min)	(ml/min)	(microns)	gap (microns)	(in. H2O)	Comment
3b	Baytron	30	22	13.2	11.4	75	5	Min. Vacuum noted
4a	Baytron	20	12	7.2	9.3	75	4	Min. Vacuum noted
4b	Baytron	20	12	7.2	9.3	50	4	Min. Vacuum noted
5a	Baytron	20	12	7.2	9.3	50	5	Streaks and Mottle
5b	Baytron	20	15	9	11.6	75	5	Increased gap improved appearance
6a	Baytron	20	15	9	11.6	100	5	better appearance (no streaks), but edges aren't holding, still have mottle
6b	Baytron	20	15	9	11.6	125	5	broke bead, rechecked gap with 3 mil shim
7a	Baytron	20	15	9	11.6	100	3.5	good quality
7b	Baytron	20	15	9	11.6	100	4.5	sucking edges
7c	Baytron	20	15	9	11.6	125	----	Could not form bead
Roll #2								
8	Baytron	20	15	9	11.6	100	3.5-4.0	made several hundred feet.
9	Bay. W/ 10% IPA	20	15	9	11.6	100	3.75	Mottle appears the same, coated several hundred feet
11	Bay. W/ 10% IPA and Zonyl	20	15	9	11.6	100	3.75	Could not establish film bead
12	Bay. W/ 10% IPA and Zonyl	20	15	9	11.6	75	3.5-4.0	Very narrow coating window, could not coat out side vacuum range given, Coated several hundred feet
Roll #3								
13a	Orgacon	20	15	low suc-tion	11.6	75	----	Could not form bead, stripes to break
13b	Orgacon	20	15	low suc-tion	11.6	62	----	Could not form bead, stripes to feathering @ 4.0"
TRIAL DATA					Calc. Wet			

Trial #	Solution	Web Speed (fpm)	Pump Set (ml/min)	Calc. Flow (ml/min)	Thickness (microns)	Die to Film gap (microns)	Vacuum (in. H_2O)	Comment
13d	Orgacon	20	15	9	11.6	44	4.25" min	Changed bottle position on inlet
13e	Orgacon	20	15	9	11.6	68	---	Could not form bead
14	Orgacon	20	15	9	11.6	56	4	Pretty good quality -- coated several hundred feet
	2nd Pass -- coated LEP polymer over 1st pass material							
Roll #3								
15/14	1% LEP	20	15	9	11.6	75	2	266F, AQ filter, suspect low flow tilted bottle
16/14	1% LEP	20	15	9	11.6	63	2.25	Still not coating well
17a/14	1% LEP	20	15	9	11.6	100	1	2 streaks, no pump pressure
17b/14	1% LEP	20	15	9	11.6	100	2	Starting to lose edges - have fix air compressor to go above 2"
18a/14	1% LEP	20	15	9	11.6	88	2	streaks
18b/14	1% LEP	20	15	9	11.6	88	2.25	OK
18c/14	1% LEP	20	15	9	11.6	88	2.5	losing bead
19/14	1% LEP	20	15	9	11.6	75	2	OK, coat hundred feet, remainder of roll #3
20/bare web	1% LEP	20	15	9	11.6	75	2	
Roll #2								
21/12	1% LEP	20	15	9	11.6	75	2	200F, almost coated w/o vacuum, no colored stripe
22a/12	1% LEP	20	12	7.2	9.3	75	2	
22b/12	1% LEP	20	15	9	11.6	50	2	Streaking
23/9	1% LEP	20	15	9	11.6	75	2	reestablished coating
24/9	1% LEP	20	15	9	11.6	63	2.5	2.25 vacuum was minimum, had 2" wide streak

								running down the center
TRIAL DATA					Calc. Wet			
		Web Speed	Pump Set	Calc. Flow	Thickness	Die to Film	Vacuum	
Trial #	Solution	(fpm)	(ml/min)	(ml/min)	(microns)	gap (microns)	(in. H2O)	Comment
25/8	1% LEP	20	15	9	11.6	63	2.25	barely stable - broke into streaks at the end
26/8	1% LEP	20	15	9	11.6	75	1.75	still have 2" band down center
27/8	1% LEP	20	15	9	11.6	75	1.5	
28/8	1% LEP	20	13	7.8	10.1	75	1.5	Minimum flow - streaks starting
29a/8	1% LEP	20	18	10.8	14.0	75	1.5	streaks visible
29b/8	1% LEP	20	18	10.8	14.0	75	2.5	stable
29c/8	1% LEP	20	18	10.8	14.0	75	2	streaks visible
30/8	1% LEP	20	13	7.8	10.1	88	2	Coating different over bare film, peppery ap-pearance, bubbles?, like little dust particles

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APPENDIX I.

Experimental Data for Offset Printing

Table I 1 MEGTEC Trial Log

	MEGTEC #1 Trial Run Data											
	Sample #	Solution	Line Speed(LS) (ft/min)	Corona Setting (KW)	Engraved Roll Ratio % of LS	Engraved Roll Direction (For/Rev)	Gravure Ratio % of LS	Gravure Direction (For/Rev)	Comments	Dot Analysis	Stripe Analysis	Engraved Patch Analysis
	1	PVA	20	0.37	1.1	For	1.1	For				
	2	PVA	20	0.37	0.998	For	1	For	Little to zero coating in stripe areas		X	
	4	PVA	20	0.37	0.998	Rev	1	For	Excellent coating quality, 1 repellancy in a 3' section, all non-engraved patches have light start and heavy trailing edges		X	
									Coat Weight builds as cell volume gets higher, but coating not as uniform as non-engraved stripe			X
	6	PVA	10	0	0.998	For	1.2	For	Stripe is coating, Coat wt. Is questionable, dimples in coating caused by extra flow?		X	
									75-95% Screen pattern looks OK, and below that see dimples			X
									Dots OK down to 200 um	X		
	7	PVA	10	0	0.998	For	1.2	Rev	Higher box pressure has increased the amount of fluid being transfer to unacceptable high levels.			
									Stripe had real heavy non-uniform edges	X		
									Best coating on sample, but still some dimple pattern			X
	8	PVA	10	0	0.998	For	1	Rev	100 um dot visible	X		
									Continuous coating from 30-100%			X
	9	PVA	10	0	0.998	For	1	For	100 um dot visible	X		
									Continuous coating from 30-100%			X
	10	PVA	10	0	1	Rev	1	For	Very good continuous coating of stripe, better than #4		X	
	11	PVA	10	0	1.2	Rev	1	For				
	12	PVA	10	0	1.2	Rev	1.2	For				
	13	PVA	10	0	1.2	Rev	2	For				
	14	PVA	10	0	2	Rev	2	For				
	15	PVA	10	0	1	For	0.67	For				
	15A	PVA	100	0	1	For	0.67	For				
	16	PVA	10	0	1	Rev	0.67	For				
	17	PVA	10	0	1	Rev	0.5	For				

Table I 1 Cont'd

Sample #	Solution	Line Speed(LS) (ft/min)	Corona Setting (KW)	Engraved Roll Ratio (% of LS)	Engraved Roll Direction (For/Rev)	Gravure Ratio (% of LS)	Gravure Direction (For/Rev)	Comments	Dot Analysis	Stripe Analysis	Engraved Patch Analysis
MEGTEC #1 Trial Run Data											
18	PVA	10	0	0.7	Rev	0.5	For				
20	Baytron	20	0.4	0.998	For	1	For				
21	Baytron	20	0.6	0.998	For	1	Rev				
22	Baytron	20	0.6	0.998	For	1.2	Rev				
23	Baytron	20	0.6	0.998	Rev	1.2	For				
24	Baytron	20	0.6	2	Rev	1.2	For				
25	Baytron	20	0.6	2	Rev	2	For	Some Repellancies		X	
26	Baytron	20	0.6	1	Rev	2	For	Some Repellancies, edge holding within 1 mm.		X	
27	Baytron	20	0.6	0.998	For	2	For	100 um dots visible, 300 um look best	X		
28	Baytron	20	1.5	1.5	For	2	For	Only edges of the stripes visible		X	
								Dots form continuous line	X		
A		20	0.3	Dyne level range achieved on PET approx. 50							
B		20	0.6	Dyne level range achieved on PET of 54-58							
C		20	0	Dyne level range achieved on PET approx. 42							
30	PVK	10	0	0.998	For	1	For	Repellancy of coating from film give meaningless data			
31	PVK	10	0	0.998	For	2	For	" " " " " " " " " " " " " " " " "			
32	PVK	10	0	0.998	For	0.6	For	" " " " " " " " " " " " " " " " "			
33	PVK	10	0	0.998	Rev	0.6	For	" " " " " " " " " " " " " " " " "			
34	PVK	15	0	0.998	Rev	1	For	" " " " " " " " " " " " " " " " "			
35	PVK	15	0	0.998	Rev	1	For	" " " " " " " " " " " " " " " " "			
36	PVK	15	0	0.998	Rev	2	For	" " " " " " " " " " " " " " " " "			
37	PVK	15	0	2	Rev	2	For	" " " " " " " " " " " " " " " " "			
38	PVK	15	0	2	Rev	1	For	" " " " " " " " " " " " " " " " "			
39	PVK	15	0	2	Rev	1	For	" " " " " " " " " " " " " " " " "			
40	PVK	15	0	0.9	Rev	1	For	" " " " " " " " " " " " " " " " "			
41	PVK	15	0	0.6	Rev	1	For	" " " " " " " " " " " " " " " " "			
			NEW FILM - MELINEX W/ ADHESION PROMOTER					" " " " " " " " " " " " " " " " "			
42	PVK	15	0	0.6	Rev	1	For	" " " " " " " " " " " " " " " " "			
43	PVK	15	0	0.6	For	1	For	" " " " " " " " " " " " " " " " "			
44	PVK	15	0	0.998	For	1	For	" " " " " " " " " " " " " " " " "			
45	PVK	15	0	0.998	For	1	For	" " " " " " " " " " " " " " " " "			
46	PVK	ramp to 50	0	0.998	For	1	Rev	" " " " " " " " " " " " " " " " "			

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APPENDIX J.

Permeation Rate of H_2O and O_2 through Alien Barrier Film

MOCON®

CONSULTING AND TESTING SERVICES (ITI#1148)
Test Report for Alien Technology Corporation

Submitted to:
Zhidan Tolt, Alien Technology Corporation
18410 Butterfield Blvd. Ste 150, Morgan Hill, CA 95037

We are pleased to present the test results for your materials submitted under:
PO#: **6530** Dated: **7/19/02**

Part A: OTR Result

Test Conditions & Results:

Permeant: 100% O_2 dry, 1 atm
Carrier Gas: 100% Nitrogen, dry, 1 atm Temperature: 23C
Instrument: MOCON Ox-Tran 2/20 (conforms to ASTM D-3985)

Sample Name	Replicate	Oxygen Transmission Rate (cc/m^2-day)
Alien Technology Coated Film	1	0.027
	2	0.021

Part B: WVTR Result

Test Conditions & Results:

Permeant: 100% RH moisture vapor at 23C (21.068mmHg)
Carrier Gas: 100% Nitrogen, dry, 1 atm Temperature: 23C
Instrument: MOCON Permatran 3/31 (conforms to ASTM F-1249)

Sample Name	Replicate	Water Vapor Transmission Rate (g/m^2-day)
Alien Technology Coated Film	1	Less than 0.005
	2	Less than 0.005

0.005 g/m^2-day is the lowest detectable level of Permatran W 3/31. Samples have been tested on-line for 150 hours

Project Scientist: J. Georgia Gu	Date: August 5, 2002

MOCON/ MODERN CONTROLS, INC. 7500 BOONE AVENUE NORTH, MINNEAPOLIS, MN 55428 U.S.A.
TEL: (763) 493-6370 FAX: (763) 493-6358

LIST OF TERMS AND ABBREVIATIONS

Baytron	A conductive polymer manufactured by Bayer, based on PEDOT
ETL	Electron Transport Layer in OLED/PLED devices
ESD	Electrostatic Discharge
FSA	Fluidic Self-Assembly. A process during which the NanoBlock ICs are distributed to specific locations on the substrate (receptor sites) from a NanoBlock IC slurry.
GreenK Emitter	Green LEP manufactured by Dow Chemical
HTL	Hole Transport Layer in OLED/PLED devices
ITO	Indium tin oxide
Jade	A NanoBlock IC used for direct drive of PLED displays
LEP	Light emitting polymer (typically a conjugated one)
NanoBlock IC, NB	Electronic circuitry on Si die with top (active) surface larger than the bottom surface (i.e., having trapezoidal cross section), used in FSA process.
NOAxxx	An optical adhesive manufactured by Norland Products, Inc.
Ogxxx	Epoxy manufactured by Epotek, Inc.
OLED	Organic Light Emitting Diode using small molecule polymers
Orgacon	A conductive polymer manufactured by Agfa, based on PEDOT
PEDOT	Polyethylenedioxythiophene; a conductive polymer
PLED	Organic Light Emitting Diode using conjugated polymers
PVA	Polyvinyl alcohol
SOG	Spin on glass
SU-x	Photoresists manufactured by Microchem, Inc
Tencor	Stylus profilometer made by Tencor
TH	Temperature-humidity (usually in reference to a stress test)
TV-1, TV-2	Codes designating internal Alien Test Vehicle structures
WYKO	Surface profiler based on interferrometry, manufactured by Veeco
Zircon	A NanoBlock IC used to drive liquid crystal display media
Zonyl	A class of fluorosurfactancts manufactured by Dupont